

EXHIBIT B

SAMSUNG CONSTRUCTIONS

Samsung Defendants' Proposed Constructions of Disputed Claim Terms and Supporting Evidence

The below chart includes Samsung's claim constructions, intrinsic evidence, and extrinsic evidence. Samsung reserves the right to rely on any evidence disclosed by Micron or Netlist in their chart of claim constructions, intrinsic evidence, and extrinsic evidence. Inclusion of evidence as extrinsic below, such as IPR proceedings, does not preclude the same evidence from being considered as intrinsic evidence.

'417 Patent

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
1	'417: 1	<p>Preamble:</p> <p>"A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the memory bus including address and control signal lines and data signal lines,</p>	<p>The preamble is limiting.</p> <p><u>Intrinsic Evidence</u></p> <p><u>U.S. Patent No. 11093417</u></p> <p>1:54-63; 2:34-46; 2:65-3:6; 5:65-6:12; 6:35-50; 7:4-9; 7:40-60; 7:61-8:9; 8:10-32; 8:33-58; 8:59-9:6; 9:7-36; 10:5-30; 10:31-43; 10:44-52; 13:26-45; 13:45-59; 13:60-67; 14:25-36; 15:48-61; 16:31-48; 16:49-17:5; 17:16-24; 17:35-43; 17:44-18:3; 18:4-18; 18:19-35; 19:56-20:3; 20:44-21:9; 21:66-22:14; 22:15-25; 22:26-35; 22:36-62; 23:12-21; 24:26-41; 24:42-54; 24:55-25:3; 25:4-26:6; 26:7-14; 29:21-30:22; 31:29-44; 31:35-32:30; 32:61-33:6; 35:1-28; 38:18-37; 41:39-51; Figs. 1, 2, 3A, 3B, 4A, 4B, 8A, 8B, 8C, 8D, 9A, 9B, 10A, 10B, 17A, 17B.</p> <p><u>File Histories</u>¹</p>

¹ Reference to a file history is intended to refer to all papers in the file history, including but not limited to non-final and final office actions, applicant/examiner interviews, terminal disclaimers, applicant responses to all office actions, amendments, and requests for continued examination.

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
		the memory module comprising:"	<p>File histories of U.S. Patents: No. 11093417, No. 7286436, No. 7289386, No. 7532537, No. 7619912, No. 7636274, No. 8154901, No. 8001434, No. 8417870, No. 7864627, No. 7881150, No. 8516185, No. 7965578, No. 8081535, No. 7916574, No. 7965579, No. 8072837, No. 8081536, No. 8081537, No. 8359501, No. 8756364, No. 8516188, No. 8787060, No. 8782350, No. 8689064, No. 9128632, No. 9606907, No. 9037774, No. 10217523, No. 9037809, No. 9318160, No. 9858215, No. 9846659, No. 10902886, No. 10860506, No. 10489314, No. 10268608, No. 10290328, No. 10949339, No. 9824035, No. 9659601, No. 9563587, No. 10025731, No. 61409893</p> <p>File histories of U.S. Patent Applications: No. 2022/0208233, No. 2021/0382834, No. 2021/0271593, No. 2021/0149829, No. 2019/0295675, No. 2021/0225415</p> <p><u>Inter Partes Reviews²</u></p> <p>IPR2014-00882 (<i>see, e.g.</i>, POPR (Paper 9) at 5, 17), IPR2014-00883 (<i>see, e.g.</i>, POPR (Paper 8) at 5-7, 15; POR (Paper 25) at 26), IPR2014-00970, IPR2014-00971, IPR2014-01011, IPR2014-01029, IPR2014-01369, IPR2014-01370, IPR2014-01371, IPR2014-01372, IPR2014-01373, IPR2014-01374, IPR2014-01375, IPR2015-01020, IPR2015-01021, IPR2017-00548, IPR2017-00549, IPR2017-00560, IPR2017-00561, IPR2017-00562, IPR2017-00577, IPR2017-00587, IPR2017-00667, IPR2017-00668, IPR2017-00692, IPR2017-00730, IPR2018-00303, IPR2018-00362, IPR2018-00363, IPR2018-00364, IPR2018-00365, IPR2020-01042, IPR2020-01044, IPR2020-01421, IPR2022-00062, IPR2022-00063, IPR2022-00064, IPR2022-00236, IPR2022-00237, IPR2022-00615, IPR2022-00639, IPR2022-00711, IPR2022-00744, IPR2022-00745, IPR2022-00996, IPR2022-00999, IPR2022-01427, IPR2022-01428, IPR2023-00203, IPR2023-</p>

² Reference to an *Inter Partes* Review (IPR) is intended to refer to all papers associated with the IPR, including but not limited to the petition, patent owner preliminary response, patent owner response, petitioner reply, patent owner sur-reply, institution decision, final written decision, and all exhibits.

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			<p>00204, IPR2023-00205, IPR2023-00405, IPR2023-00406, IPR2023-00454, IPR2023-00455, IPR2023-00847, IPR2023-00883</p> <p><u>Inter Partes Reexaminations</u>³</p> <p>No. 95/000546, No. 95/000577, No. 95/000578, No. 95/000579, No. 95/001337, No. 95/001339, No. 95/001381, No. 95/001758</p> <p><u>Federal Circuit Appeals</u>⁴</p> <p>No. 15-126, No. 15-1179, No. 16-1742 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-1743 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-1744 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-2274, No. 16-2666, No. 17-1617, No. 17-1618, No. 18-1676, No. 18-2034, No. 18-2036, No. 18-2037, No. 18-2123, No. 18-2357, No. 19-1720, No. 19-2340, No. 20-1026, No. 21-113, No. 21-114</p> <p><u>Extrinsic Evidence</u></p> <p><u>District Court Cases</u>⁵</p>

³ Reference to an *Inter Partes* Reexamination is intended to refer to all papers associated with the reexamination, including but not limited to all non-final and final actions, patent owner responses, briefs, communications, and exhibits.

⁴ Reference to a Federal Circuit appeal is intended to refer to all materials associated with the appeal, including but not limited to briefs, motions, replies, orders, decisions, and appendices.

⁵ Reference to a district court case is intended to refer to all materials associated with the litigation, including but not limited to briefs, pleadings, motions, disclosures, replies, orders, decisions, and appendices.

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
			<p>No. 2:09-cv-06900 (C.D. Cal.), No. 8:13-cv-00996 (C.D. Cal.), No. 8:16-cv-01605 (C.D. Cal.), No. 8:17-cv-01030 (C.D. Cal.), No. 2:12-cv-02319 (E.D. Cal.), No. 2:13-cv-02613 (E.D. Cal.), No. 3:09-cv-05718 (N.D. Cal.), No. 4:08-cv-04144 (N.D. Cal.), No. 4:13-cv-03901 (N.D. Cal.), No. 4:13-cv-03916 (N.D. Cal.), No. 4:13-cv-05889 (N.D. Cal.), No. 4:13-cv-05962 (N.D. Cal.), No. 5:22-mc-80337 (N.D. Cal.), No. 1:09-cv-00165 (D. Del.), No. 1:21-cv-01453 (D. Del.), No. 2:21-cv-00463 (E.D. Tex.), No. 2:22-cv-00203 (E.D. Tex.), No. 2:22-cv-00294 (E.D. Tex.), No. 1:22-cv-00134 (W.D. Tex.), No. 1:22-cv-00136 (W.D. Tex.), No. 6:20-cv-00194 (W.D. Tex.), No. 6:20-cv-00525 (W.D. Tex.), No. 6:21-cv-00430 (W.D. Tex.), No. 6:21-cv-00431 (W.D. Tex.)</p> <p><u>International Trade Commission Investigations</u>⁶</p> <p>No. 337-TA-1023, No. 337-TA-1089</p> <p><u>Others</u></p> <p>JEDEC Standards: JEDEC Standard No. 21C, JESD 79-4 Standard, JEDEC 82-31A Standard, JEDEC 82-32A Standard, JESD 248A Standard, JEDEC 79-4C Standard, JESD 79 Standard, JESD 79-2 Standard</p> <p>Memory Systems: Cache, DRAM, Disk (Bruce Jacob) (2008)</p> <p>Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob) (December 10, 2002)</p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '417 patent</p>

⁶ Reference to an International Trade Commission (ITC) Investigation is intended to refer to all materials associated with the ITC investigation, including but not limited to briefs, motions, replies, orders, decisions, and appendices.

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			<p>was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p> <p>Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.</p>
2	'417: 1	"operable in a computer system to communicate data"	<p>"configured in a computer system to communicate data"</p> <p><u>Intrinsic Evidence</u></p> <p><u>U.S. Patent No. 11093417</u></p> <p>1:54-63; 2:34-46; 2:65-3:6; 5:65-6:12; 6:35-50; 7:4-9; 7:40-60; 7:61-8:9; 8:10-32; 8:59-9:6; 9:7-36; 10:5-30; 10:31-43; 10:44-52; 13:26-45; 13:45-59; 13:60-67; 14:25-36; 15:48-61; 16:31-48; 17:16-24; 17:35-43; 17:44-18:3; 18:4-18; 18:19-35; 19:56-20:3; 20:44-21:9; 21:66-22:14; 22:15-25; 22:26-35; 22:36-62; 23:12-21; 24:26-41; 24:42-54; 24:55-25:3; 25:4-26:6; 26:7-14; 29:21-30:22; 31:29-44; 31:35-32:30; 32:61-33:6; 35:2-28; 38:18-37; 41:39-51; Figs. 1, 2, 3A, 3B, 4A, 4B, 8A, 8B, 9A, 9B, 17A, 17B.</p> <p><u>File Histories</u></p> <p>File histories of U.S. Patents: No. 11093417, No. 7286436, No. 7289386, No. 7532537, No. 7619912, No. 7636274, No. 8154901, No. 8001434, No. 8417870, No. 7864627, No. 7881150, No. 8516185, No. 7965578, No. 8081535, No. 7916574, No. 7965579, No. 8072837, No. 8081536, No. 8081537, No. 8359501, No. 8756364, No. 8516188, No. 8787060, No. 8782350, No. 8689064, No. 9128632, No. 9606907, No. 9037774, No. 10217523, No. 9037809, No. 9318160, No. 9858215, No. 9846659, No. 10902886, No.</p>

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			<p>10860506, No. 10489314, No. 10268608, No. 10290328, No. 10949339, No. 9824035, No. 9659601, No. 9563587, No. 10025731, No. 61409893</p> <p>File histories of U.S. Patent Applications: No. 2022/0208233, No. 2021/0382834, No. 2021/0271593, No. 2021/0149829, No. 2019/0295675, No. 2021/0225415</p> <p><u>Inter Partes Reviews</u></p> <p>IPR2014-00882 (<i>see, e.g.</i>, POPR (Paper 9) at 5, 17), IPR2014-00883 (<i>see, e.g.</i>, POPR (Paper 8) at 5-7, 15; POR (Paper 25) at 26), IPR2014-00970, IPR2014-00971, IPR2014-01011, IPR2014-01029, IPR2014-01369, IPR2014-01370, IPR2014-01371, IPR2014-01372, IPR2014-01373, IPR2014-01374, IPR2014-01375, IPR2015-01020, IPR2015-01021, IPR2017-00548, IPR2017-00549, IPR2017-00560, IPR2017-00561, IPR2017-00562, IPR2017-00577, IPR2017-00587, IPR2017-00667, IPR2017-00668, IPR2017-00692, IPR2017-00730, IPR2018-00303, IPR2018-00362, IPR2018-00363, IPR2018-00364, IPR2018-00365, IPR2020-01042, IPR2020-01044, IPR2020-01421, IPR2022-00062, IPR2022-00063, IPR2022-00064, IPR2022-00236, IPR2022-00237, IPR2022-00615, IPR2022-00639, IPR2022-00711, IPR2022-00744, IPR2022-00745, IPR2022-00996, IPR2022-00999, IPR2022-01427, IPR2022-01428, IPR2023-00203, IPR2023-00204, IPR2023-00205, IPR2023-00405, IPR2023-00406, IPR2023-00454, IPR2023-00455, IPR2023-00847, IPR2023-00883</p> <p><u>Inter Partes Reexaminations</u></p> <p>No. 95/000546, No. 95/000577, No. 95/000578, No. 95/000579, No. 95/001337, No. 95/001339, No. 95/001381, No. 95/001758</p> <p><u>Federal Circuit Appeals</u></p> <p>No. 15-126, No. 15-1179, No. 16-1742 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No.</p>

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			<p>44) at 2-3), No. 16-1743 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-1744 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-2274, No. 16-2666, No. 17-1617, No. 17-1618, No. 18-1676, No. 18-2034, No. 18-2036, No. 18-2037, No. 18-2123, No. 18-2357, No. 19-1720, No. 19-2340, No. 20-1026, No. 21-113, No. 21-114</p> <p><u>Extrinsic Evidence</u></p> <p><u>District Court Cases</u></p> <p>No. 2:09-cv-06900 (C.D. Cal.), No. 8:13-cv-00996 (C.D. Cal.), No. 8:16-cv-01605 (C.D. Cal.), No. 8:17-cv-01030 (C.D. Cal.), No. 2:12-cv-02319 (E.D. Cal.), No. 2:13-cv-02613 (E.D. Cal.), No. 3:09-cv-05718 (N.D. Cal.), No. 4:08-cv-04144 (N.D. Cal.), No. 4:13-cv-03901 (N.D. Cal.), No. 4:13-cv-03916 (N.D. Cal.), No. 4:13-cv-05889 (N.D. Cal.), No. 4:13-cv-05962 (N.D. Cal.), No. 5:22-mc-80337 (N.D. Cal.), No. 1:09-cv-00165 (D. Del.), No. 1:21-cv-01453 (D. Del.), No. 2:21-cv-00463 (E.D. Tex.), No. 2:22-cv-00203 (E.D. Tex.), No. 2:22-cv-00294 (E.D. Tex.), No. 1:22-cv-00134 (W.D. Tex.), No. 1:22-cv-00136 (W.D. Tex.), No. 6:20-cv-00194 (W.D. Tex.), No. 6:20-cv-00525 (W.D. Tex.), No. 6:21-cv-00430 (W.D. Tex.), No. 6:21-cv-00431 (W.D. Tex.)</p> <p><u>International Trade Commission Investigations</u></p> <p>No. 337-TA-1023, No. 337-TA-1089</p> <p><u>Others</u></p> <p>JEDEC Standards: JEDEC Standard No. 21C, JESD 79-4 Standard, JEDEC 82-31A Standard, JEDEC 82-32A Standard, JESD 248A Standard, JEDEC 79-4C Standard, JESD 79 Standard, JESD 79-2 Standard</p>

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			<p>Memory Systems: Cache, DRAM, Disk (Bruce Jacob) (2008)</p> <p>Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob) (December 10, 2002)</p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '417 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p> <p>Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.</p>
3	'417: 1, 4, 5, 8, 10	"rank"	<p>"an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip-select signals, to read or write the full bit-width of the memory module"</p> <p><u>Intrinsic Evidence</u></p> <p><u>U.S. Patent No. 11093417</u></p> <p>2:46-53; 2:65-3:2; 6:51-58; 7:10-16; 7:61-8:9; 8:59-9:6; 9:7-18; 10:5-23; 10:44-52; 14:25-29; 14:37-46; 14:47-55; 14:56-15:4; 15:5-12; 15:13-27; 17:25-34; 17:44-18:3; 18:4-18; 18:19-35; 18:37-39; 18:56-19:10; 19:11-27; 19:28-30; 20:44-58; 21:66-22:14; 22:15-25; 22:26-35; 22:63-23:10; 31:45-32:30; 33:25-43; 33:54-34:6; 34:59-67; Tables 1, 2; Figs.1, 4A, 4B, 8A, 8B, 8C, 8D, 9A, 9B, 10A, 10B, 11A, 11B</p> <p><u>File Histories</u></p>

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#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
			<p>No. 337-TA-1023, No. 337-TA-1089</p> <p><u>Others</u></p> <p>JEDEC Standards: JEDEC Standard No. 21C, JESD 79-4 Standard, JEDEC 82-31A Standard, JEDEC 82-32A Standard, JESD 248A Standard, JEDEC 79-4C Standard, JESD 79 Standard, JESD 79-2 Standard</p> <p>Memory Systems: Cache, DRAM, Disk (Bruce Jacob) (2008)</p> <p>Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob) (December 10, 2002)</p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '417 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p> <p>Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.</p>
4	'417: 1, 3, 11	"data buffer control signals"	<p>"a signal sent to a buffer to selectively electrically couple the data signal line at the input of the buffer to a first signal line and a second signal line at the output of the buffer wherein each of the first signal line and the second signal line is connected to a different rank"</p> <p><u>Intrinsic Evidence</u></p> <p><u>U.S. Patent No. 11093417</u></p>

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
			<p>7:32-35; 9:37-50</p> <p><u>File Histories</u></p> <p>File histories of U.S. Patents: No. 11093417, No. 7286436, No. 7289386, No. 7532537, No. 7619912, No. 7636274, No. 8154901, No. 8001434, No. 8417870, No. 7864627, No. 7881150, No. 8516185, No. 7965578, No. 8081535, No. 7916574, No. 7965579, No. 8072837, No. 8081536, No. 8081537, No. 8359501, No. 8756364, No. 8516188, No. 8787060, No. 8782350, No. 8689064, No. 9128632, No. 9606907, No. 9037774, No. 10217523, No. 9037809, No. 9318160, No. 9858215, No. 9846659, No. 10902886, No. 10860506, No. 10489314, No. 10268608, No. 10290328, No. 10949339, No. 9824035, No. 9659601, No. 9563587, No. 10025731, No. 61409893</p> <p>File histories of U.S. Patent Applications: No. 2022/0208233, No. 2021/0382834, No. 2021/0271593, No. 2021/0149829, No. 2019/0295675, No. 2021/0225415</p> <p><u>Inter Partes Reviews</u></p> <p>IPR2014-00882 (<i>see, e.g.</i>, POPR (Paper 9) at 5, 17), IPR2014-00883 (<i>see, e.g.</i>, POPR (Paper 8) at 5-7, 15; POR (Paper 25) at 26), IPR2014-00970, IPR2014-00971, IPR2014-01011, IPR2014-01029, IPR2014-01369, IPR2014-01370, IPR2014-01371, IPR2014-01372, IPR2014-01373, IPR2014-01374, IPR2014-01375, IPR2015-01020, IPR2015-01021, IPR2017-00548, IPR2017-00549, IPR2017-00560, IPR2017-00561, IPR2017-00562, IPR2017-00577, IPR2017-00587, IPR2017-00667, IPR2017-00668, IPR2017-00692, IPR2017-00730, IPR2018-00303, IPR2018-00362, IPR2018-00363, IPR2018-00364, IPR2018-00365, IPR2020-01042, IPR2020-01044, IPR2020-01421, IPR2022-00062, IPR2022-00063, IPR2022-00064, IPR2022-00236, IPR2022-00237, IPR2022-00615, IPR2022-00639, IPR2022-00711, IPR2022-00744, IPR2022-00745, IPR2022-00996, IPR2022-00999, IPR2022-01427, IPR2022-01428, IPR2023-00203, IPR2023-00204, IPR2023-00205, IPR2023-00405, IPR2023-00406, IPR2023-00454, IPR2023-00455, IPR2023-00847, IPR2023-00883</p>

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
			<p data-bbox="869 358 1220 386"><u>Inter Partes Reexaminations</u></p> <p data-bbox="869 428 1906 492">No. 95/000546, No. 95/000577, No. 95/000578, No. 95/000579, No. 95/001337, No. 95/001339, No. 95/001381, No. 95/001758</p> <p data-bbox="869 532 1161 560"><u>Federal Circuit Appeals</u></p> <p data-bbox="869 602 1969 902">No. 15-126, No. 15-1179, No. 16-1742 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-1743 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-1744 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-2274, No. 16-2666, No. 17-1617, No. 17-1618, No. 18-1676, No. 18-2034, No. 18-2036, No. 18-2037, No. 18-2123, No. 18-2357, No. 19-1720, No. 19-2340, No. 20-1026, No. 21-113, No. 21-114</p> <p data-bbox="869 943 1125 971"><u>Extrinsic Evidence</u></p> <p data-bbox="869 1013 1119 1040"><u>District Court Cases</u></p> <p data-bbox="869 1083 1969 1393">No. 2:09-cv-06900 (C.D. Cal.), No. 8:13-cv-00996 (C.D. Cal.), No. 8:16-cv-01605 (C.D. Cal.), No. 8:17-cv-01030 (C.D. Cal.), No. 2:12-cv-02319 (E.D. Cal.), No. 2:13-cv-02613 (E.D. Cal.), No. 3:09-cv-05718 (N.D. Cal.), No. 4:08-cv-04144 (N.D. Cal.), No. 4:13-cv-03901 (N.D. Cal.), No. 4:13-cv-03916 (N.D. Cal.), No. 4:13-cv-05889 (N.D. Cal.), No. 4:13-cv-05962 (N.D. Cal.), No. 5:22-mc-80337 (N.D. Cal.), No. 1:09-cv-00165 (D. Del.), No. 1:21-cv-01453 (D. Del.), No. 2:21-cv-00463 (E.D. Tex.), No. 2:22-cv-00203 (E.D. Tex.), No. 2:22-cv-00294 (E.D. Tex.), No. 1:22-cv-00134 (W.D. Tex.), No. 1:22-cv-00136 (W.D. Tex.), No. 6:20-cv-00194 (W.D. Tex.), No. 6:20-cv-00525 (W.D. Tex.), No. 6:21-cv-00430 (W.D. Tex.), No. 6:21-cv-00431 (W.D. Tex.)</p>

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
			<p><u>International Trade Commission Investigations</u></p> <p>No. 337-TA-1023, No. 337-TA-1089</p> <p><u>Others</u></p> <p>JEDEC Standards: JEDEC Standard No. 21C, JESD 79-4 Standard, JEDEC 82-31A Standard, JEDEC 82-32A Standard, JESD 248A Standard, JEDEC 79-4C Standard, JESD 79 Standard, JESD 79-2 Standard</p> <p>Memory Systems: Cache, DRAM, Disk (Bruce Jacob) (2008)</p> <p>Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob) (December 10, 2002)</p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '417 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p> <p>Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.</p>
5	'417: 1	"circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide	"a data buffer coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the buffer configurable to selectively electrically couple a single data signal line at the input of the buffer to a first signal line and second signal line at the output of the buffer to transfer N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide rank, wherein each signal line at the output of the buffer is connected to a different N-bit wide rank."

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
		ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signal”	<p><u>Intrinsic Evidence</u></p> <p><u>U.S. Patent No. 11093417</u></p> <p>5:65-6:12; 6:35-43; 7:4-9; 7:32-35; 7:40-60; 7:61-8:9; 8:10-26; 8:33-58; 8:59-9:6; 9:7-36; 9:37-50; 10:5-10; 10:13-23; 10:53-57; 14:37-46; 14:47-55; 14:56-15:4; 15:5-12; 15:13-27; 15:28-40; 15:48-61; 16:31-48; 16:49-17:2; 17:-34-43; 17:44-50; 18:19-35; 18:37-39; 18:56-19:9; 19:28-30; 22:36-56; 31:59-32:30; 33:7-24; 33:25-38; 33:58-34:6; 34:24-38; Tables 1, 2; Example 1; Figs. 1, 2, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 5D, 8A, 8B, 8C, 8D, 9A, 9B, 10A, 10B, 11A</p> <p>U.S. Patent Application No. 14/715,486 at [0011]-[0013] (filed May 18, 2015)</p> <p><u>File Histories</u></p> <p>File histories of U.S. Patents: No. 11093417, No. 7286436, No. 7289386, No. 7532537, No. 7619912, No. 7636274, No. 8154901, No. 8001434, No. 8417870, No. 7864627, No. 7881150, No. 8516185, No. 7965578, No. 8081535, No. 7916574, No. 7965579, No. 8072837, No. 8081536, No. 8081537, No. 8359501, No. 8756364, No. 8516188, No. 8787060, No. 8782350, No. 8689064, No. 9128632, No. 9606907, No. 9037774, No. 10217523, No. 9037809, No. 9318160, No. 9858215, No. 9846659, No. 10902886, No. 10860506, No. 10489314, No. 10268608, No. 10290328, No. 10949339, No. 9824035, No. 9659601, No. 9563587, No. 10025731, No. 61409893</p> <p>File histories of U.S. Patent Applications: No. 2022/0208233, No. 2021/0382834, No. 2021/0271593, No. 2021/0149829, No. 2019/0295675, No. 2021/0225415</p> <p><u>Inter Partes Reviews</u></p>

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
			<p>IPR2014-00882 (<i>see, e.g.</i>, POPR (Paper 9) at 5, 17), IPR2014-00883 (<i>see, e.g.</i>, POPR (Paper 8) at 5-7, 15; POR (Paper 25) at 26), IPR2014-00970, IPR2014-00971, IPR2014-01011, IPR2014-01029, IPR2014-01369, IPR2014-01370, IPR2014-01371, IPR2014-01372, IPR2014-01373, IPR2014-01374, IPR2014-01375, IPR2015-01020, IPR2015-01021, IPR2017-00548, IPR2017-00549, IPR2017-00560, IPR2017-00561, IPR2017-00562, IPR2017-00577, IPR2017-00587, IPR2017-00667, IPR2017-00668, IPR2017-00692, IPR2017-00730, IPR2018-00303, IPR2018-00362, IPR2018-00363, IPR2018-00364, IPR2018-00365, IPR2020-01042, IPR2020-01044, IPR2020-01421, IPR2022-00062, IPR2022-00063, IPR2022-00064, IPR2022-00236, IPR2022-00237, IPR2022-00615, IPR2022-00639, IPR2022-00711, IPR2022-00744, IPR2022-00745, IPR2022-00996, IPR2022-00999, IPR2022-01427, IPR2022-01428, IPR2023-00203, IPR2023-00204, IPR2023-00205, IPR2023-00405, IPR2023-00406, IPR2023-00454, IPR2023-00455, IPR2023-00847, IPR2023-00883</p> <p><u>Inter Partes Reexaminations</u></p> <p>No. 95/000546, No. 95/000577, No. 95/000578, No. 95/000579, No. 95/001337, No. 95/001339, No. 95/001381, No. 95/001758</p> <p><u>Federal Circuit Appeals</u></p> <p>No. 15-126, No. 15-1179, No. 16-1742 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-1743 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-1744 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-2274, No. 16-2666, No. 17-1617, No. 17-1618, No. 18-1676, No. 18-2034, No. 18-2036, No. 18-2037, No. 18-2123, No. 18-2357, No. 19-1720, No. 19-2340, No. 20-1026, No. 21-113, No. 21-114</p>

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
			<p><u>Extrinsic Evidence</u></p> <p><u>District Court Cases</u></p> <p>No. 2:09-cv-06900 (C.D. Cal.), No. 8:13-cv-00996 (C.D. Cal.), No. 8:16-cv-01605 (C.D. Cal.), No. 8:17-cv-01030 (C.D. Cal.), No. 2:12-cv-02319 (E.D. Cal.), No. 2:13-cv-02613 (E.D. Cal.), No. 3:09-cv-05718 (N.D. Cal.), No. 4:08-cv-04144 (N.D. Cal.), No. 4:13-cv-03901 (N.D. Cal.), No. 4:13-cv-03916 (N.D. Cal.), No. 4:13-cv-05889 (N.D. Cal.), No. 4:13-cv-05962 (N.D. Cal.), No. 5:22-mc-80337 (N.D. Cal.), No. 1:09-cv-00165 (D. Del.), No. 1:21-cv-01453 (D. Del.), No. 2:21-cv-00463 (E.D. Tex.), No. 2:22-cv-00203 (E.D. Tex.), No. 2:22-cv-00294 (E.D. Tex.), No. 1:22-cv-00134 (W.D. Tex.), No. 1:22-cv-00136 (W.D. Tex.), No. 6:20-cv-00194 (W.D. Tex.), No. 6:20-cv-00525 (W.D. Tex.), No. 6:21-cv-00430 (W.D. Tex.), No. 6:21-cv-00431 (W.D. Tex.)</p> <p><u>International Trade Commission Investigations</u></p> <p>No. 337-TA-1023, No. 337-TA-1089</p> <p><u>Others</u></p> <p>JEDEC Standards: JEDEC Standard No. 21C, JESD 79-4 Standard, JEDEC 82-31A Standard, JEDEC 82-32A Standard, JESD 248A Standard, JEDEC 79-4C Standard, JESD 79 Standard, JESD 79-2 Standard</p> <p>Memory Systems: Cache, DRAM, Disk (Bruce Jacob) (2008)</p> <p>Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob) (December 10, 2002)</p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '417 patent</p>

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
			<p>was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p> <p>Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.</p>
6	'417: 6, 11	<p>"circuitry includes logic pipelines configurable to enable the data transfers between the memory devices and the memory bus through the circuitry"</p> <p>"circuitry is configurable to enable the data paths in response to the data buffer control signals so that the burst of N-bit wide data signals are transferred via the data paths"</p>	<p>Plain and ordinary meaning.</p> <p><u>Intrinsic Evidence</u></p> <p><u>U.S. Patent No. 11093417</u></p> <p>9:37-43; 10:5-23; 13:41-56; 22:36-62; 23:4-10; 37:43-48; Figs. 3A, 3B, 4A, 4B</p> <p><u>Extrinsic Evidence</u></p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '417 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p> <p>Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.</p>
7	'417: 1	<p>"logic . . . configurable to receive a set of input address and control signals</p>	<p>Plain and ordinary meaning.</p> <p><u>Intrinsic Evidence</u></p>

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
		associated with a read or write memory command via the address and control signal lines and to output a set of registered address and control signals in response to the set of input address and control signals, . . . the logic is further configurable to output data buffer control signals in response to the read or write memory command”	<p><u>U.S. Patent No. 11093417</u></p> <p>7:17-31; 7:32-35; 9:37-50; 10:53-57; 14:25-29;16:31-48; 16:49-17:5; 17:35-43; 18:19-35; 22:9-14; 22:20-25; Example 1; Figs. 3A, 3B, 4A, 4B, 9A, 9B</p> <p><u>Extrinsic Evidence</u></p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '417 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p> <p>Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.</p>
8	'417: 1, 15	“the read or write command”	<p>“the read or write memory command”</p> <p><u>Intrinsic Evidence</u></p> <p><u>U.S. Patent No. 11093417</u></p> <p>2:65-3:4; 8:26-32; 13:46-59; 19:11-24; 19:51-53; 22:53-56; 23:4-10; 25:4-26:3; 35:13-15; Table 2; Figs. 6A, 6B</p> <p><u>Extrinsic Evidence</u></p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '417 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p>

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
			Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.
9	'417: 9	"the predetermined amount of time delay"	<p>Plain and ordinary meaning.</p> <p><u>Intrinsic Evidence</u></p> <p><u>U.S. Patent No. 11093417</u></p> <p>16:55-58; 22:41-56; 38:45-51; 39:25-28</p> <p><u>Extrinsic Evidence</u></p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '417 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p> <p>Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.</p>
10	'417: 1	"overall CAS latency of the memory module"	<p>Plain and ordinary meaning.</p> <p><u>Intrinsic Evidence</u></p> <p><u>U.S. Patent No. 11093417</u></p>

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
			<p>22:36-60; Example 2</p> <p><u>Extrinsic Evidence</u></p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '417 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p> <p>Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.</p>
11	'417: 1	"actual operational CAS latency of each of the memory devices"	<p>Plain and ordinary meaning.</p> <p><u>Intrinsic Evidence</u></p> <p><u>U.S. Patent No. 11093417</u></p> <p>22:36-60; Example 2</p> <p><u>Extrinsic Evidence</u></p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '417 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p>

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
			Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.
12	'417: 1	"wherein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices"	<p>Plain and ordinary meaning.</p> <p><u>Intrinsic Evidence</u></p> <p>22:36-60; 38:45-51; Example 2</p> <p><u>Extrinsic Evidence</u></p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '417 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p> <p>Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.</p>

'215 Patent

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
13	'215: 1, 21	<p>Preambles:</p> <p>“A memory module operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst, the memory module comprising:”; and</p> <p>“A method of operating a memory module coupled to a memory controller via a memory bus, the memory</p>	<p>The preambles are limiting.</p> <p><u>Intrinsic Evidence</u></p> <p><u>U.S. Patent No. 9858215</u></p> <p>1:42-45; 1:47-53; 2:28-36; 2:59-67; 5:18-32; 5:55-63; 6:24-39; 6:60-7:13; 7:14-29; 7:30-39; 8:12-14; 8:27-33; 9:18-35; 9:43-55; 9:56-64; 11:49-55; 11:66-12:4; 12:5-12; 12:13-21; 13:36-49; 14:19-36; 15:4-11; 15:21-29; 15:30-36; 15:46-51; 15:57-16:3; 16:4-11; 17:50-56; 18:55-62; 19:52-67; 20:1-11; 20:12-21; 20:22-24; 22:29-39; 22:42-53; 22:58-64; 23:10-16; 25:38-40; 26:62-65; 27:10-26; 27:67-28:5; 30:5-10; 33:23-29; 36:44-54; Figs. 1, 2, 3A, 3B, 4A, 4B, 8A, 8B, 8C, 8D, 9A, 9B, 10A, 10B, 17A, 17B</p> <p><u>File Histories</u></p> <p>File histories of U.S. Patents: No. 9858215, No. 7286436, No. 7289386, No. 7532537, No. 7619912, No. 7636274, No. 8154901, No. 8001434, No. 8417870, No. 7864627, No. 7881150, No. 8516185, No. 7965578, No. 8081535, No. 7916574, No. 7965579, No. 8072837, No. 8081536, No. 8081537, No. 8359501, No. 8756364, No. 8516188, No. 8787060, No. 8782350, No. 8689064, No. 9128632, No. 9606907, No. 9037774, No. 10217523, No. 9037809, No. 11093417, No. 9318160, No. 9846659, No. 10902886, No. 10860506, No. 10489314, No. 10268608, No. 10290328, No. 10949339, No. 9824035, No. 9659601, No. 9563587, No. 10025731, No. 61409893</p> <p>File histories of U.S. Patent Applications: No. 2022/0208233, No. 2021/0382834, No. 2021/0271593, No. 2021/0149829, No. 2019/0295675, No. 2021/0225415</p> <p><u>Inter Partes Reviews</u></p>

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		module comprising memory integrated circuits arranged in ranks and mounted on a printed circuit board having a plurality of edge connections coupled to the memory bus, the memory integrated circuits including at least one first memory integrated circuit in a first rank and at least one second memory integrated circuit in a second rank, the method comprising:"	<p>IPR2014-00882 (<i>see, e.g.</i>, POPR (Paper 9) at 5, 17), IPR2014-00883 (<i>see, e.g.</i>, POPR (Paper 8) at 5-7, 15; POR (Paper 25) at 26), IPR2014-00970, IPR2014-00971, IPR2014-01011, IPR2014-01029, IPR2014-01369, IPR2014-01370, IPR2014-01371, IPR2014-01372, IPR2014-01373, IPR2014-01374, IPR2014-01375, IPR2015-01020, IPR2015-01021, IPR2017-00548, IPR2017-00549, IPR2017-00560, IPR2017-00561, IPR2017-00562, IPR2017-00577, IPR2017-00587, IPR2017-00667, IPR2017-00668, IPR2017-00692, IPR2017-00730, IPR2018-00303, IPR2018-00362, IPR2018-00363, IPR2018-00364, IPR2018-00365, IPR2020-01042, IPR2020-01044, IPR2020-01421, IPR2022-00062, IPR2022-00063, IPR2022-00064, IPR2022-00236, IPR2022-00237, IPR2022-00615, IPR2022-00639, IPR2022-00711, IPR2022-00744, IPR2022-00745, IPR2022-00996, IPR2022-00999, IPR2022-01427, IPR2022-01428, IPR2023-00203, IPR2023-00204, IPR2023-00205, IPR2023-00405, IPR2023-00406, IPR2023-00454, IPR2023-00455, IPR2023-00847, IPR2023-00883</p> <p><u>Inter Partes Reexaminations</u></p> <p>No. 95/000546, No. 95/000577, No. 95/000578, No. 95/000579, No. 95/001337, No. 95/001339, No. 95/001381, No. 95/001758</p> <p><u>Federal Circuit Appeals</u></p> <p>No. 15-126, No. 15-1179, No. 16-1742 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-1743 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-1744 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-2274, No. 16-2666, No. 17-1617, No. 17-1618, No. 18-1676, No. 18-2034, No. 18-2036, No. 18-2037, No. 18-2123, No. 18-2357, No. 19-1720, No. 19-2340, No. 20-1026, No. 21-113, No. 21-114</p>

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			<p><u>Extrinsic Evidence</u></p> <p><u>District Court Cases</u></p> <p>No. 2:09-cv-06900 (C.D. Cal.), No. 8:13-cv-00996 (C.D. Cal.), No. 8:16-cv-01605 (C.D. Cal.), No. 8:17-cv-01030 (C.D. Cal.), No. 2:12-cv-02319 (E.D. Cal.), No. 2:13-cv-02613 (E.D. Cal.), No. 3:09-cv-05718 (N.D. Cal.), No. 4:08-cv-04144 (N.D. Cal.), No. 4:13-cv-03901 (N.D. Cal.), No. 4:13-cv-03916 (N.D. Cal.), No. 4:13-cv-05889 (N.D. Cal.), No. 4:13-cv-05962 (N.D. Cal.), No. 5:22-mc-80337 (N.D. Cal.), No. 1:09-cv-00165 (D. Del.), No. 1:21-cv-01453 (D. Del.), No. 2:21-cv-00463 (E.D. Tex.), No. 2:22-cv-00203 (E.D. Tex.), No. 2:22-cv-00294 (E.D. Tex.), No. 1:22-cv-00134 (W.D. Tex.), No. 1:22-cv-00136 (W.D. Tex.), No. 6:20-cv-00194 (W.D. Tex.), No. 6:20-cv-00525 (W.D. Tex.), No. 6:21-cv-00430 (W.D. Tex.), No. 6:21-cv-00431 (W.D. Tex.)</p> <p><u>International Trade Commission Investigations</u></p> <p>No. 337-TA-1023, No. 337-TA-1089</p> <p><u>Others</u></p> <p>JEDEC Standards: JEDEC Standard No. 21C, JEDEC 79-4C Standard, JEDEC 82-31A Standard, JEDEC 79-4-1B Standard, JEDEC 82-32A Standard, JEDEC 79-4C Standard, JESD 79 Standard, JESD 79-2 Standard</p> <p>Memory Systems: Cache, DRAM, Disk (Bruce Jacob) (2008)</p> <p>Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob) (December 10, 2002)</p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '215 patent</p>

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			<p>was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p> <p>Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.</p>
14	'215: 1, 14, 21, 26	"rank"	<p>"an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip-select signals, to read or write the full bit-width of the memory module"</p> <p><u>Intrinsic Evidence</u></p> <p><u>U.S. Patent No. 9858215</u></p> <p>2:41-47; 2:59-63; 6:9-11; 6:30-36; 7:14-29; 8:12-26; 8:27-38; 9:18-35; 9:56-64; 12:13-17; 12:25-34; 12:35-43; 12:44-59; 12:60-67; 13:1-15; 15:30-56; 15:57-16:3; 16:4-20; 16:22-24; 16:42-62; 16:63-17:12; 17:13-15; 18:30-44; 19:52-67; 20:1-11; 20:12-21; 20:49-63; 20:64-21:6; 22:24-28; 22:35-41; 22:47-57; 27:10-33; 28:27-45; 28:56-29:8; 29:29:27-41; Tables 1, 2; Figs.1, 4A, 4B, 8A, 8B, 8C, 8D, 9A, 9B, 10A, 10B, 11A, 11B</p> <p><u>File Histories</u></p> <p>File histories of U.S. Patents: No. 9858215, No. 7286436, No. 7289386, No. 7532537, No. 7619912, No. 7636274, No. 8154901, No. 8001434, No. 8417870, No. 7864627, No. 7881150, No. 8516185, No. 7965578, No. 8081535, No. 7916574, No. 7965579, No. 8072837, No. 8081536, No. 8081537, No. 8359501, No. 8756364, No. 8516188, No. 8787060, No. 8782350, No. 8689064, No. 9128632, No. 9606907, No. 9037774, No. 10217523, No. 9037809, No. 11093417, No. 9318160, No. 9846659, No. 10902886, No.</p>

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			<p>10860506, No. 10489314, No. 10268608, No. 10290328, No. 10949339, No. 9824035, No. 9659601, No. 9563587, No. 10025731, No. 61409893</p> <p>File histories of U.S. Patent Applications: No. 2022/0208233, No. 2021/0382834, No. 2021/0271593, No. 2021/0149829, No. 2019/0295675, No. 2021/0225415</p> <p><u>Inter Partes Reviews</u></p> <p>IPR2014-00882 (<i>see, e.g.</i>, POPR (Paper 9) at 5, 17), IPR2014-00883 (<i>see, e.g.</i>, POPR (Paper 8) at 5-7, 15; POR (Paper 25) at 26), IPR2014-00970, IPR2014-00971, IPR2014-01011, IPR2014-01029, IPR2014-01369, IPR2014-01370, IPR2014-01371, IPR2014-01372, IPR2014-01373, IPR2014-01374, IPR2014-01375, IPR2015-01020, IPR2015-01021, IPR2017-00548, IPR2017-00549, IPR2017-00560, IPR2017-00561, IPR2017-00562, IPR2017-00577, IPR2017-00587, IPR2017-00667, IPR2017-00668, IPR2017-00692, IPR2017-00730, IPR2018-00303, IPR2018-00362, IPR2018-00363, IPR2018-00364, IPR2018-00365, IPR2020-01042, IPR2020-01044, IPR2020-01421, IPR2022-00062, IPR2022-00063, IPR2022-00064, IPR2022-00236, IPR2022-00237, IPR2022-00615, IPR2022-00639, IPR2022-00711, IPR2022-00744, IPR2022-00745, IPR2022-00996, IPR2022-00999, IPR2022-01427, IPR2022-01428, IPR2023-00203, IPR2023-00204, IPR2023-00205, IPR2023-00405, IPR2023-00406, IPR2023-00454, IPR2023-00455, IPR2023-00847, IPR2023-00883</p> <p><u>Inter Partes Reexaminations</u></p> <p>No. 95/000546, No. 95/000577, No. 95/000578, No. 95/000579, No. 95/001337, No. 95/001339, No. 95/001381, No. 95/001758</p> <p><u>Federal Circuit Appeals</u></p> <p>No. 15-126, No. 15-1179, No. 16-1742 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No.</p>

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			<p>44) at 2-3), No. 16-1743 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-1744 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-2274, No. 16-2666, No. 17-1617, No. 17-1618, No. 18-1676, No. 18-2034, No. 18-2036, No. 18-2037, No. 18-2123, No. 18-2357, No. 19-1720, No. 19-2340, No. 20-1026, No. 21-113, No. 21-114</p> <p><u>Extrinsic Evidence</u></p> <p><u>District Court Cases</u></p> <p>No. 2:09-cv-06900 (C.D. Cal.), No. 8:13-cv-00996 (C.D. Cal.), No. 8:16-cv-01605 (C.D. Cal.), No. 8:17-cv-01030 (C.D. Cal.), No. 2:12-cv-02319 (E.D. Cal.), No. 2:13-cv-02613 (E.D. Cal.), No. 3:09-cv-05718 (N.D. Cal.), No. 4:08-cv-04144 (N.D. Cal.), No. 4:13-cv-03901 (N.D. Cal.), No. 4:13-cv-03916 (N.D. Cal.), No. 4:13-cv-05889 (N.D. Cal.), No. 4:13-cv-05962 (N.D. Cal.), No. 5:22-mc-80337 (N.D. Cal.), No. 1:09-cv-00165 (D. Del.), No. 1:21-cv-01453 (D. Del.), No. 2:21-cv-00463 (E.D. Tex.), No. 2:22-cv-00203 (E.D. Tex.), No. 2:22-cv-00294 (E.D. Tex.), No. 1:22-cv-00134 (W.D. Tex.), No. 1:22-cv-00136 (W.D. Tex.), No. 6:20-cv-00194 (W.D. Tex.), No. 6:20-cv-00525 (W.D. Tex.), No. 6:21-cv-00430 (W.D. Tex.), No. 6:21-cv-00431 (W.D. Tex.)</p> <p><u>International Trade Commission Investigations</u></p> <p>No. 337-TA-1023, No. 337-TA-1089</p> <p><u>Others</u></p> <p>JEDEC Standards: JEDEC Standard No. 21C, JEDEC 79-4C Standard, JEDEC 82-31A Standard, JEDEC 79-4-1B Standard, JEDEC 82-32A Standard, JEDEC 79-4C Standard, JESD 79 Standard, JESD 79-2 Standard</p>

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			<p>Memory Systems: Cache, DRAM, Disk (Bruce Jacob) (2008)</p> <p>Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob) (December 10, 2002)</p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '215 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p> <p>Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.</p>
15	'215: 1	"operable in a computer system to communicate data"	<p>"configured in a computer system to communicate data"</p> <p><u>Intrinsic Evidence</u></p> <p><u>U.S. Patent No. 9858215</u></p> <p>1:47-53; 2:28-36; 2:59-67; 5:18-32; 5:55-63; 6:24-39; 6:60-7:13; 7:14-29; 7:30-39; 8:12-14; 8:27-33; 9:18-35; 9:43-55; 9:56-64; 11:49-55; 11:66-12:4; 12:5-12; 12:13-21; 13:36-49; 14:19-36; 15:4-11; 15:21-29; 15:30-36; 15:46-51; 15:57-16:3; 16:4-11; 17:50-56; 18:55-62; 19:52-67; 20:1-11; 20:12-21; 20:22-24; 22:29-39; 22:42-53; 22:58-64; 23:10-16; 25:38-40; 26:62-65; 27:10-26; 27:67-28:5; 30:5-10; 33:23-29; 36:44-54; Examples 2, 3; Figs. 1, 2, 3A, 3B, 4A, 4B, 8A, 8B, 8C, 8D, 9A, 9B, 10A, 10B, 17A, 17B</p> <p><u>File Histories</u></p>

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			<p>2037, No. 18-2123, No. 18-2357, No. 19-1720, No. 19-2340, No. 20-1026, No. 21-113, No. 21-114</p> <p><u>Others</u></p> <p>JEDEC Standards: JEDEC Standard No. 21C, JEDEC 79-4C Standard, JEDEC 82-31A Standard, JEDEC 79-4-1B Standard, JEDEC 82-32A Standard, JEDEC 79-4C Standard, JESD 79 Standard, JESD 79-2 Standard</p> <p>Memory Systems: Cache, DRAM, Disk (Bruce Jacob) (2008)</p> <p>Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob) (December 10, 2002)</p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '215 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p> <p>Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.</p>
16	'215: 1, 21	"logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at	"logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to selectively electrically couple the input of the buffer to a first data signal line at the output of the data buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer, and disabling a second data signal line at the output of the buffer connected to the second memory integrated circuit"

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		<p>least one first memory integrated circuit and the memory controller through the buffer”; and</p> <p>“in response to the first memory command, providing first control signals to a buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer”</p>	<p>“in response to the first memory command, providing first control signals to selectively electrically couple the input of the buffer to a first data signal line at the output of the data buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer, and disabling a second data signal line at the output of the buffer connected to the second memory integrated circuit”</p> <p><u>Intrinsic Evidence</u></p> <p><u>U.S. Patent No. 9858215</u></p> <p>5:18-32; 5:55-63; 6:24-29; 6:37-43; 6:48-51; 6:52-55; 6:60-7:13; 7:14-29; 7:30-52; 7:53-8:11; 8:12-26; 8:27-56; 8:57-9:3; 9:18-35; 9:65-10:2; 12:25-34; 25:35-43; 12:44-59; 12:60-67; 13:1-15; 13:16-28; 13:36-49; 14:19-36; 14:37-57; 15:21-29; 16:4-20; 16:42-62; 17:13-15; 19:62-67; 20:1-11; 22:19-28; 22:49-57; 27:24-33; 28:9-23; 28:27-45; 28:63-29:8; 29:27-35; Tables 1, 2; Example 1; Figs. 1, 2, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 5D, 8A, 8B, 8C, 8D, 9A, 9B, 10A, 10B, 11A</p> <p>U.S. Patent Application No. 14/715,486 at [0011]-[0013] (filed May 18, 2015)</p> <p><u>File Histories</u></p> <p>File histories of U.S. Patents: No. 9858215, No. 7286436, No. 7289386, No. 7532537, No. 7619912, No. 7636274, No. 8154901, No. 8001434, No. 8417870, No. 7864627, No. 7881150, No. 8516185, No. 7965578, No. 8081535, No. 7916574, No. 7965579, No. 8072837, No. 8081536, No. 8081537, No. 8359501, No. 8756364, No. 8516188, No. 8787060, No. 8782350, No. 8689064, No. 9128632, No. 9606907, No. 9037774, No. 10217523, No. 9037809, No. 11093417, No. 9318160, No. 9846659, No. 10902886, No. 10860506, No. 10489314, No. 10268608, No. 10290328, No. 10949339, No. 9824035, No. 9659601, No. 9563587, No. 10025731, No. 61409893</p>

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
			<p>File histories of U.S. Patent Applications: No. 2022/0208233, No. 2021/0382834, No. 2021/0271593, No. 2021/0149829, No. 2019/0295675, No. 2021/0225415</p> <p><u>Inter Partes Reviews</u></p> <p>IPR2014-00882 (<i>see, e.g.</i>, POPR (Paper 9) at 5, 17), IPR2014-00883 (<i>see, e.g.</i>, POPR (Paper 8) at 5-7, 15; POR (Paper 25) at 26), IPR2014-00970, IPR2014-00971, IPR2014-01011, IPR2014-01029, IPR2014-01369, IPR2014-01370, IPR2014-01371, IPR2014-01372, IPR2014-01373, IPR2014-01374, IPR2014-01375, IPR2015-01020, IPR2015-01021, IPR2017-00548, IPR2017-00549, IPR2017-00560, IPR2017-00561, IPR2017-00562, IPR2017-00577, IPR2017-00587, IPR2017-00667, IPR2017-00668, IPR2017-00692, IPR2017-00730, IPR2018-00303, IPR2018-00362, IPR2018-00363, IPR2018-00364, IPR2018-00365, IPR2020-01042, IPR2020-01044, IPR2020-01421, IPR2022-00062, IPR2022-00063, IPR2022-00064, IPR2022-00236, IPR2022-00237, IPR2022-00615, IPR2022-00639, IPR2022-00711, IPR2022-00744, IPR2022-00745, IPR2022-00996, IPR2022-00999, IPR2022-01427, IPR2022-01428, IPR2023-00203, IPR2023-00204, IPR2023-00205, IPR2023-00405, IPR2023-00406, IPR2023-00454, IPR2023-00455, IPR2023-00847, IPR2023-00883</p> <p><u>Inter Partes Reexaminations</u></p> <p>No. 95/000546, No. 95/000577, No. 95/000578, No. 95/000579, No. 95/001337, No. 95/001339, No. 95/001381, No. 95/001758</p> <p><u>Federal Circuit Appeals</u></p> <p>No. 15-126, No. 15-1179, No. 16-1742 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-1743 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No.</p>

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
			<p>16-1744 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-2274, No. 16-2666, No. 17-1617, No. 17-1618, No. 18-1676, No. 18-2034, No. 18-2036, No. 18-2037, No. 18-2123, No. 18-2357, No. 19-1720, No. 19-2340, No. 20-1026, No. 21-113, No. 21-114</p> <p><u>Extrinsic Evidence</u></p> <p><u>District Court Cases</u></p> <p>No. 2:09-cv-06900 (C.D. Cal.), No. 8:13-cv-00996 (C.D. Cal.), No. 8:16-cv-01605 (C.D. Cal.), No. 8:17-cv-01030 (C.D. Cal.), No. 2:12-cv-02319 (E.D. Cal.), No. 2:13-cv-02613 (E.D. Cal.), No. 3:09-cv-05718 (N.D. Cal.), No. 4:08-cv-04144 (N.D. Cal.), No. 4:13-cv-03901 (N.D. Cal.), No. 4:13-cv-03916 (N.D. Cal.), No. 4:13-cv-05889 (N.D. Cal.), No. 4:13-cv-05962 (N.D. Cal.), No. 5:22-mc-80337 (N.D. Cal.), No. 1:09-cv-00165 (D. Del.), No. 1:21-cv-01453 (D. Del.), No. 2:21-cv-00463 (E.D. Tex.), No. 2:22-cv-00203 (E.D. Tex.), No. 2:22-cv-00294 (E.D. Tex.), No. 1:22-cv-00134 (W.D. Tex.), No. 1:22-cv-00136 (W.D. Tex.), No. 6:20-cv-00194 (W.D. Tex.), No. 6:20-cv-00525 (W.D. Tex.), No. 6:21-cv-00430 (W.D. Tex.), No. 6:21-cv-00431 (W.D. Tex.)</p> <p><u>International Trade Commission Investigations</u></p> <p>No. 337-TA-1023, No. 337-TA-1089</p> <p><u>Others</u></p> <p>JEDEC Standards: JEDEC Standard No. 21C, JEDEC 79-4C Standard, JEDEC 82-31A Standard, JEDEC 79-4-1B Standard, JEDEC 82-32A Standard, JEDEC 79-4C Standard, JESD 79 Standard, JESD 79-2 Standard</p> <p>Memory Systems: Cache, DRAM, Disk (Bruce Jacob) (2008)</p>

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
			<p>Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob) (December 10, 2002)</p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '215 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p> <p>Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.</p>
17	'215: 1, 21	<p>"wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals"; and</p> <p>"in response to the second memory command,</p>	<p>"wherein logic is further configured to respond to the second memory command by providing second control signals to selectively electrically couple the input of the buffer to a second data signal line at the output of the data buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, and disabling a first data signal line at the output of the buffer connected to the first memory integrated circuit"</p> <p>"in response to the second memory command, providing second control signals to selectively electrically couple the input of the buffer to a second data signal line at the output of the data buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, and disabling a first data signal line at the output of the buffer connected to the first memory integrated circuit"</p> <p><u>Intrinsic Evidence</u></p>

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
		providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals”	<p><u>U.S. Patent No. 9858215</u></p> <p>5:18-32; 5:55-63; 6:24-29; 6:37-43; 6:48-51; 6:52-55; 6:60-7:13; 7:14-29; 7:30-52; 7:53-8:11; 8:12-26; 8:27-56; 8:57-9:3; 9:18-35; 9:65-10:2; 12:25-34; 25:35-43; 12:44-59; 12:60-67; 13:1-15; 13:16-28; 13:36-49; 14:19-36; 14:37-57; 15:21-29; 16:4-20; 16:42-62; 17:13-15; 19:62-67; 20:1-11; 22:19-28; 22:49-57; 27:24-33; 28:9-23; 28:27-45; 28:63-29:8; 29:27-35; Tables 1, 2; Example 1; Figs. 1, 2, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 5D, 8A, 8B, 8C, 8D, 9A, 9B, 10A, 10B, 11A</p> <p>U.S. Patent Application No. 14/715,486 at [0011]-[0013] (filed May 18, 2015)</p> <p><u>File Histories</u></p> <p>File histories of U.S. Patents: No. 9858215, No. 7286436, No. 7289386, No. 7532537, No. 7619912, No. 7636274, No. 8154901, No. 8001434, No. 8417870, No. 7864627, No. 7881150, No. 8516185, No. 7965578, No. 8081535, No. 7916574, No. 7965579, No. 8072837, No. 8081536, No. 8081537, No. 8359501, No. 8756364, No. 8516188, No. 8787060, No. 8782350, No. 8689064, No. 9128632, No. 9606907, No. 9037774, No. 10217523, No. 9037809, No. 11093417, No. 9318160, No. 9846659, No. 10902886, No. 10860506, No. 10489314, No. 10268608, No. 10290328, No. 10949339, No. 9824035, No. 9659601, No. 9563587, No. 10025731, No. 61409893</p> <p>File histories of U.S. Patent Applications: No. 2022/0208233, No. 2021/0382834, No. 2021/0271593, No. 2021/0149829, No. 2019/0295675, No. 2021/0225415</p> <p><u>Inter Partes Reviews</u></p> <p>IPR2014-00882 (<i>see, e.g.</i>, POPR (Paper 9) at 5, 17), IPR2014-00883 (<i>see, e.g.</i>, POPR (Paper 8) at 5-7, 15; POR (Paper 25) at 26), IPR2014-00970, IPR2014-00971, IPR2014-01011, IPR2014-01029, IPR2014-01369, IPR2014-01370, IPR2014-01371, IPR2014-01372, IPR2014-01373, IPR2014-01374, IPR2014-01375, IPR2015-01020, IPR2015-</p>

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
			<p>01021, IPR2017-00548, IPR2017-00549, IPR2017-00560, IPR2017-00561, IPR2017-00562, IPR2017-00577, IPR2017-00587, IPR2017-00667, IPR2017-00668, IPR2017-00692, IPR2017-00730, IPR2018-00303, IPR2018-00362, IPR2018-00363, IPR2018-00364, IPR2018-00365, IPR2020-01042, IPR2020-01044, IPR2020-01421, IPR2022-00062, IPR2022-00063, IPR2022-00064, IPR2022-00236, IPR2022-00237, IPR2022-00615, IPR2022-00639, IPR2022-00711, IPR2022-00744, IPR2022-00745, IPR2022-00996, IPR2022-00999, IPR2022-01427, IPR2022-01428, IPR2023-00203, IPR2023-00204, IPR2023-00205, IPR2023-00405, IPR2023-00406, IPR2023-00454, IPR2023-00455, IPR2023-00847, IPR2023-00883</p> <p><u>Inter Partes Reexaminations</u></p> <p>No. 95/000546, No. 95/000577, No. 95/000578, No. 95/000579, No. 95/001337, No. 95/001339, No. 95/001381, No. 95/001758</p> <p><u>Federal Circuit Appeals</u></p> <p>No. 15-126, No. 15-1179, No. 16-1742 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-1743 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-1744 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-2274, No. 16-2666, No. 17-1617, No. 17-1618, No. 18-1676, No. 18-2034, No. 18-2036, No. 18-2037, No. 18-2123, No. 18-2357, No. 19-1720, No. 19-2340, No. 20-1026, No. 21-113, No. 21-114</p> <p><u>Extrinsic Evidence</u></p> <p><u>District Court Cases</u></p>

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
			<p>No. 2:09-cv-06900 (C.D. Cal.), No. 8:13-cv-00996 (C.D. Cal.), No. 8:16-cv-01605 (C.D. Cal.), No. 8:17-cv-01030 (C.D. Cal.), No. 2:12-cv-02319 (E.D. Cal.), No. 2:13-cv-02613 (E.D. Cal.), No. 3:09-cv-05718 (N.D. Cal.), No. 4:08-cv-04144 (N.D. Cal.), No. 4:13-cv-03901 (N.D. Cal.), No. 4:13-cv-03916 (N.D. Cal.), No. 4:13-cv-05889 (N.D. Cal.), No. 4:13-cv-05962 (N.D. Cal.), No. 5:22-mc-80337 (N.D. Cal.), No. 1:09-cv-00165 (D. Del.), No. 1:21-cv-01453 (D. Del.), No. 2:21-cv-00463 (E.D. Tex.), No. 2:22-cv-00203 (E.D. Tex.), No. 2:22-cv-00294 (E.D. Tex.), No. 1:22-cv-00134 (W.D. Tex.), No. 1:22-cv-00136 (W.D. Tex.), No. 6:20-cv-00194 (W.D. Tex.), No. 6:20-cv-00525 (W.D. Tex.), No. 6:21-cv-00430 (W.D. Tex.), No. 6:21-cv-00431 (W.D. Tex.)</p> <p><u>International Trade Commission Investigations</u></p> <p>No. 337-TA-1023, No. 337-TA-1089</p> <p><u>Others</u></p> <p>JEDEC Standards: JEDEC Standard No. 21C, JEDEC 79-4C Standard, JEDEC 82-31A Standard, JEDEC 79-4-1B Standard, JEDEC 82-32A Standard, JEDEC 79-4C Standard, JESD 79 Standard, JESD 79-2 Standard</p> <p>Memory Systems: Cache, DRAM, Disk (Bruce Jacob) (2008)</p> <p>Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob) (December 10, 2002)</p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '215 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p>

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
			Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.
18	'215: 3, 4, 24, 25	"the memory module has an overall CAS latency" / "overall CAS latency of the memory module"	<p>Plain and ordinary meaning.</p> <p><u>Intrinsic Evidence</u></p> <p><u>U.S. Patent No. 9858215</u></p> <p>20:22-47; Example 2</p> <p><u>Extrinsic Evidence</u></p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '215 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p> <p>Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.</p>
19	'215: 3, 4, 24, 25	"actual operational CAS latency of each of the plurality of memory integrated circuits" / "actual operational CAS latency of the memory integrated circuits"	<p>Plain and ordinary meaning.</p> <p><u>Intrinsic Evidence</u></p> <p><u>U.S. Patent No. 9858215</u></p> <p>20:22-47; Example 2</p>

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
			<p><u>Extrinsic Evidence</u></p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '215 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p> <p>Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.</p>
20	'215 patent: 12, 13, 28, 29	"burst of data strobe signals"	<p>Plain and ordinary meaning.</p> <p><u>Intrinsic Evidence</u></p> <p><u>U.S. Patent No. 9858215</u></p> <p>11:40-57; 11:58-66; 12:35-43; 12:44-59; 13:1-15; Figs. 6A, 8A, 8B</p> <p><u>Extrinsic Evidence</u></p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '215 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p> <p>Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.</p>

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
21	'215: 15	"the at least one of the circuit components"	<p>Plain and ordinary meaning.</p> <p><u>Intrinsic Evidence</u></p> <p><u>U.S. Patent No. 9858215</u></p> <p>5:18-32; 5:33-43; 5:55-63; 6:24-29; 6:37-43; 6:48-51; 6:52-55; 6:60-7:13; 7:14-29; 7:30-52; 7:53-8:11; 8:12-26; 8:27-56; 8:57-9:3; 9:18-35; 9:65-10:2; 12:25-34; 25:35-43; 12:44-59; 12:60-67; 13:1-15; 13:16-28; 13:36-49; 14:19-36; 14:37-60; 14:61-15:3; 15:4-11; 15:21-29; 16:4-20; 16:42-62; 17:13-15; 19:62-67; 20:1-11; 22:19-28; 22:49-57; 27:24-33; 28:9-23; 28:27-45; 28:63-29:8; 29:27-35; 35:37-45; Tables 1, 2; Example 1; Figs. 1, 2, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 5D, 8A, 8B, 8C, 8D, 9A, 9B, 10A, 10B, 11A</p> <p><u>Extrinsic Evidence</u></p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '215 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p> <p>Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.</p>

'912 Patent

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
22	'912: All asserted claims	"rank"	<p data-bbox="821 396 1978 493">"an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip select signals, to read or write the full bit-width of the memory module."</p> <p data-bbox="821 526 1073 558"><u>Intrinsic Evidence</u></p> <p data-bbox="821 599 1129 631"><u>U.S. Patent No. 7619912</u></p> <p data-bbox="821 667 1934 732">2:16-42; 2:59-3:14; 6:31-38; 6:55-9:21; 12:11-23:25; 23:60-24:38; 25:27-44; 32:27-38; Figs 1A, 1B, 2A, 2B, 3A, 3B, 11A, 11B.</p> <p data-bbox="821 768 1978 833">JEDEC standard JESD79D, "Double Data Rate (DDR) SDRAM Specification." published February 2004.</p> <p data-bbox="821 873 989 906"><u>File Histories</u></p> <p data-bbox="821 946 1934 1222">File histories of U.S. Patents: No. 7619912, No. 7286436, No. 7289386, No. 7532537, No. 7636274, No. 8154901, No. 8001434, No. 8417870, No. 7864627, No. 7881150, No. 8516185, No. 7965578, No. 8081535, No. 7916574, No. 7965579, No. 8072837, No. 8081536, No. 8081537, No. 8359501, No. 8756364, No. 8516188, No. 8787060, No. 8782350, No. 8689064, No. 9128632, No. 9606907, No. 9037774, No. 10217523, No. 9037809, No. 9318160, No. 9858215, No. 9846659, No. 11093417, No. 10902886, No. 10860506, No. 10489314, No. 10268608, No. 10290328, No. 10949339, No. 9824035, No. 9659601, No. 9563587, No. 10025731, No. 61409893</p> <p data-bbox="821 1263 1871 1328">File histories of U.S. Patent Applications: No. 2022/0208233, No. 2021/0382834, No. 2021/0271593, No. 2021/0149829, No. 2019/0295675, No. 2021/0225415</p> <p data-bbox="821 1369 1083 1401"><u>Inter Partes Reviews</u></p>

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
			<p>IPR2014-00882 (<i>see, e.g.</i>, POPR (Paper 9) at 5, 17), IPR2014-00883 (<i>see, e.g.</i>, POPR (Paper 8) at 5-7, 15; POR (Paper 25) at 26), IPR2014-00970, IPR2014-00971, IPR2014-01011, IPR2014-01029, IPR2014-01369, IPR2014-01370, IPR2014-01371, IPR2014-01372, IPR2014-01373, IPR2014-01374, IPR2014-01375, IPR2015-01020, IPR2015-01021, IPR2017-00548, IPR2017-00549, IPR2017-00560, IPR2017-00561, IPR2017-00562, IPR2017-00577, IPR2017-00587, IPR2017-00667, IPR2017-00668, IPR2017-00692, IPR2017-00730, IPR2018-00303, IPR2018-00362, IPR2018-00363, IPR2018-00364, IPR2018-00365, IPR2020-01042, IPR2020-01044, IPR2020-01421, IPR2022-00062, IPR2022-00063, IPR2022-00064, IPR2022-00236, IPR2022-00237, IPR2022-00615, IPR2022-00639, IPR2022-00711, IPR2022-00744, IPR2022-00745, IPR2022-00996, IPR2022-00999, IPR2022-01427, IPR2022-01428, IPR2023-00203, IPR2023-00204, IPR2023-00205, IPR2023-00405, IPR2023-00406, IPR2023-00454, IPR2023-00455, IPR2023-00847, IPR2023-00883</p> <p><u>Inter Partes Reexaminations</u></p> <p>No. 95/000546, No. 95/000577, No. 95/000578, No. 95/000579, No. 95/001337, No. 95/001339, No. 95/001381, No. 95/001758</p> <p><u>Federal Circuit Appeals</u></p> <p>No. 15-126, No. 15-1179, No. 16-1742 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-1743 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-1744 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-2274, No. 16-2666, No. 17-1617, No. 17-1618, No. 18-1676, No. 18-2034, No. 18-2036, No. 18-2037, No. 18-2123, No. 18-2357, No. 19-1720, No. 19-2340, No. 20-1026, No. 21-113, No. 21-114</p>

			<p><u>Extrinsic Evidence</u></p> <p><u>District Court Cases</u></p> <p>No. 2:09-cv-06900 (C.D. Cal.), No. 8:13-cv-00996 (C.D. Cal.), No. 8:16-cv-01605 (C.D. Cal.), No. 8:17-cv-01030 (C.D. Cal.), No. 2:12-cv-02319 (E.D. Cal.), No. 2:13-cv-02613 (E.D. Cal.), No. 3:09-cv-05718 (N.D. Cal.), No. 4:08-cv-04144 (N.D. Cal.), No. 4:13-cv-03901 (N.D. Cal.), No. 4:13-cv-03916 (N.D. Cal.), No. 4:13-cv-05889 (N.D. Cal.), No. 4:13-cv-05962 (N.D. Cal.), No. 5:22-mc-80337 (N.D. Cal.), No. 1:09-cv-00165 (D. Del.), No. 1:21-cv-01453 (D. Del.), No. 2:21-cv-00463 (E.D. Tex.), No. 2:22-cv-00203 (E.D. Tex.), No. 2:22-cv-00294 (E.D. Tex.), No. 1:22-cv-00134 (W.D. Tex.), No. 1:22-cv-00136 (W.D. Tex.), No. 6:20-cv-00194 (W.D. Tex.), No. 6:20-cv-00525 (W.D. Tex.), No. 6:21-cv-00430 (W.D. Tex.), No. 6:21-cv-00431 (W.D. Tex.)</p> <p><u>International Trade Commission Investigations</u></p> <p>No. 337-TA-1023, No. 337-TA-1089</p> <p><u>Others</u></p> <p>JEDEC Standards: JESD 205 Standard, JESD 82-20A Standard, JESD 206 Standard, JESD 79-2F Standard, JEDEC Standard No. 21C, JEDEC No. 21C Specification for DDR3 LRDIMM, JESD 82-30 Standard, JESD 79-3F Standard, JESD 248A Standard, JESD 79-4 Standard, JESD 82-31A Standard, JESD 79-4-1B Standard, JESD 79-4C Standard</p> <p>Memory Systems: Cache, DRAM, Disk (Bruce Jacob) (2008)</p> <p>Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob) (December 10, 2002)</p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '912 patent was filed,</p>
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#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
			<p>the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p> <p>Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.</p>
23	'912: All Asserted Claims	"row[/column] address signal"	<p>"a varying electrical impulse that conveys an address of either a row or a column of memory locations from one point to another"</p> <p><u>Intrinsic Evidence</u></p> <p><u>U.S. Patent No. 7619912</u></p> <p>5:22-45; 6:55-64; 7:36-11:42; 12:11-20:63; 21:13-22:63; Figures 1A, 1B, 2A, 2B, 3A, and 3B.</p> <p>JEDEC standard JESD79D, "Double Data Rate (DDR) SDRAM Specification." published February 2004.</p> <p><u>File Histories</u></p> <p>File histories of U.S. Patents: No. 7619912, No. 7286436, No. 7289386, No. 7532537, No. 7636274, No. 8154901, No. 8001434, No. 8417870, No. 7864627, No. 7881150, No. 8516185, No. 7965578, No. 8081535, No. 7916574, No. 7965579, No. 8072837, No. 8081536, No. 8081537, No. 8359501, No. 8756364, No. 8516188, No. 8787060, No. 8782350, No. 8689064, No. 9128632, No. 9606907, No. 9037774, No. 10217523, No. 9037809, No. 9318160, No. 9858215, No. 9846659, No. 11093417, No. 10902886, No. 10860506, No. 10489314, No. 10268608, No. 10290328, No. 10949339, No. 9824035, No. 9659601, No. 9563587, No. 10025731, No. 61409893</p>

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			<p>No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-2274, No. 16-2666, No. 17-1617, No. 17-1618, No. 18-1676, No. 18-2034, No. 18-2036, No. 18-2037, No. 18-2123, No. 18-2357, No. 19-1720, No. 19-2340, No. 20-1026, No. 21-113, No. 21-114</p> <p><u>Extrinsic Evidence</u></p> <p><u>District Court Cases</u></p> <p>No. 2:09-cv-06900 (C.D. Cal.), No. 8:13-cv-00996 (C.D. Cal.), No. 8:16-cv-01605 (C.D. Cal.), No. 8:17-cv-01030 (C.D. Cal.), No. 2:12-cv-02319 (E.D. Cal.), No. 2:13-cv-02613 (E.D. Cal.), No. 3:09-cv-05718 (N.D. Cal.), No. 4:08-cv-04144 (N.D. Cal.), No. 4:13-cv-03901 (N.D. Cal.), No. 4:13-cv-03916 (N.D. Cal.), No. 4:13-cv-05889 (N.D. Cal.), No. 4:13-cv-05962 (N.D. Cal.), No. 5:22-mc-80337 (N.D. Cal.), No. 1:09-cv-00165 (D. Del.), No. 1:21-cv-01453 (D. Del.), No. 2:21-cv-00463 (E.D. Tex.), No. 2:22-cv-00203 (E.D. Tex.), No. 2:22-cv-00294 (E.D. Tex.), No. 1:22-cv-00134 (W.D. Tex.), No. 1:22-cv-00136 (W.D. Tex.), No. 6:20-cv-00194 (W.D. Tex.), No. 6:20-cv-00525 (W.D. Tex.), No. 6:21-cv-00430 (W.D. Tex.), No. 6:21-cv-00431 (W.D. Tex.)</p> <p><u>International Trade Commission Investigations</u></p> <p>No. 337-TA-1023, No. 337-TA-1089</p> <p><u>Others</u></p> <p>JEDEC Standards: JESD 205 Standard, JESD 82-20A Standard, JESD 206 Standard, JESD 79-2F Standard, JEDEC Standard No. 21C, JEDEC No. 21C Specification for DDR3 LRDIMM, JESD 82-30 Standard, JESD 79-3F Standard, JESD 248A Standard, JESD 79-4 Standard, JESD 82-31A Standard, JESD 79-4-1B Standard, JESD 79-4C Standard</p> <p>Memory Systems: Cache, DRAM, Disk (Bruce Jacob) (2008)</p>

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			<p>Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob) (December 10, 2002)</p> <p>The Penguin Dictionary of Electronics ("signal")</p> <p>Collins Dictionary Electronics: Definitions for the Digital Age ("signal")</p> <p>Microsoft Computer Dictionary, Fifth edition 2002 ("signal")</p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '912 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p> <p>Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.</p>
24	'912: 15, 16, 28, 86, 88	"coupled to the printed circuit board"	<p>"electrically connected to the printed circuit board."</p> <p><u>Intrinsic Evidence</u></p> <p><u>U.S. Patent No. 7619912</u></p> <p>2:45-59; 3:15-29; 5:6-55; 6:4-11; 21:36-24:58; 25:26-44; 26:2-28; 28:13-24; 28:45-58; 29:1-30; 30:22-31:23; 31:56-32:3; Figures 1A, 1B, 2A, 2B, 3A, 11A, 11B</p> <p>JEDEC standard JESD79D, "Double Data Rate (DDR) SDRAM Specification." published February 2004.</p> <p><u>File Histories</u></p>

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			<p>File histories of U.S. Patents: No. 7619912, No. 7286436, No. 7289386, No. 7532537, No. 7636274, No. 8154901, No. 8001434, No. 8417870, No. 7864627, No. 7881150, No. 8516185, No. 7965578, No. 8081535, No. 7916574, No. 7965579, No. 8072837, No. 8081536, No. 8081537, No. 8359501, No. 8756364, No. 8516188, No. 8787060, No. 8782350, No. 8689064, No. 9128632, No. 9606907, No. 9037774, No. 10217523, No. 9037809, No. 9318160, No. 9858215, No. 9846659, No. 11093417, No. 10902886, No. 10860506, No. 10489314, No. 10268608, No. 10290328, No. 10949339, No. 9824035, No. 9659601, No. 9563587, No. 10025731, No. 61409893</p> <p>File histories of U.S. Patent Applications: No. 2022/0208233, No. 2021/0382834, No. 2021/0271593, No. 2021/0149829, No. 2019/0295675, No. 2021/0225415</p> <p><u>Inter Partes Reviews</u></p> <p>IPR2014-00882 (<i>see, e.g.</i>, POPR (Paper 9) at 5, 17), IPR2014-00883 (<i>see, e.g.</i>, POPR (Paper 8) at 5-7, 15; POR (Paper 25) at 26), IPR2014-00970, IPR2014-00971, IPR2014-01011, IPR2014-01029, IPR2014-01369, IPR2014-01370, IPR2014-01371, IPR2014-01372, IPR2014-01373, IPR2014-01374, IPR2014-01375, IPR2015-01020, IPR2015-01021, IPR2017-00548, IPR2017-00549, IPR2017-00560, IPR2017-00561, IPR2017-00562, IPR2017-00577, IPR2017-00587, IPR2017-00667, IPR2017-00668, IPR2017-00692, IPR2017-00730, IPR2018-00303, IPR2018-00362, IPR2018-00363, IPR2018-00364, IPR2018-00365, IPR2020-01042, IPR2020-01044, IPR2020-01421, IPR2022-00062, IPR2022-00063, IPR2022-00064, IPR2022-00236, IPR2022-00237, IPR2022-00615, IPR2022-00639, IPR2022-00711, IPR2022-00744, IPR2022-00745, IPR2022-00996, IPR2022-00999, IPR2022-01427, IPR2022-01428, IPR2023-00203, IPR2023-00204, IPR2023-00205, IPR2023-00405, IPR2023-00406, IPR2023-00454, IPR2023-00455, IPR2023-00847, IPR2023-00883</p> <p><u>Inter Partes Reexaminations</u></p>

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			<p>No. 95/000546, No. 95/000577, No. 95/000578, No. 95/000579, No. 95/001337, No. 95/001339, No. 95/001381, No. 95/001758</p> <p><u>Federal Circuit Appeals</u></p> <p>No. 15-126, No. 15-1179, No. 16-1742 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-1743 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-1744 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-2274, No. 16-2666, No. 17-1617, No. 17-1618, No. 18-1676, No. 18-2034, No. 18-2036, No. 18-2037, No. 18-2123, No. 18-2357, No. 19-1720, No. 19-2340, No. 20-1026, No. 21-113, No. 21-114</p> <p><u>Extrinsic Evidence</u></p> <p><u>District Court Cases</u></p> <p>No. 2:09-cv-06900 (C.D. Cal.), No. 8:13-cv-00996 (C.D. Cal.), No. 8:16-cv-01605 (C.D. Cal.), No. 8:17-cv-01030 (C.D. Cal.), No. 2:12-cv-02319 (E.D. Cal.), No. 2:13-cv-02613 (E.D. Cal.), No. 3:09-cv-05718 (N.D. Cal.), No. 4:08-cv-04144 (N.D. Cal.), No. 4:13-cv-03901 (N.D. Cal.), No. 4:13-cv-03916 (N.D. Cal.), No. 4:13-cv-05889 (N.D. Cal.), No. 4:13-cv-05962 (N.D. Cal.), No. 5:22-mc-80337 (N.D. Cal.), No. 1:09-cv-00165 (D. Del.), No. 1:21-cv-01453 (D. Del.), No. 2:21-cv-00463 (E.D. Tex.), No. 2:22-cv-00203 (E.D. Tex.), No. 2:22-cv-00294 (E.D. Tex.), No. 1:22-cv-00134 (W.D. Tex.), No. 1:22-cv-00136 (W.D. Tex.), No. 6:20-cv-00194 (W.D. Tex.), No. 6:20-cv-00525 (W.D. Tex.), No. 6:21-cv-00430 (W.D. Tex.), No. 6:21-cv-00431 (W.D. Tex.)</p> <p><u>International Trade Commission Investigations</u></p> <p>No. 337-TA-1023, No. 337-TA-1089</p>

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
			<p><u>Others</u></p> <p>JEDEC Standards: JESD 205 Standard, JESD 82-20A Standard, JESD 206 Standard, JESD 79-2F Standard, JEDEC Standard No. 21C, JEDEC No. 21C Specification for DDR3 LRDIMM, JESD 82-30 Standard, JESD 79-3F Standard, JESD 248A Standard, JESD 79-4 Standard, JESD 82-31A Standard, JESD 79-4-1B Standard, JESD 79-4C Standard</p> <p>Memory Systems: Cache, DRAM, Disk (Bruce Jacob) (2008)</p> <p>Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob) (December 10, 2002)</p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '912 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p> <p>Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.</p>
25	'912: 1, 39, 77, 80, 82, 90	"mounted to the printed circuit board"	<p>"attached to the printed circuit board"</p> <p><u>Intrinsic Evidence</u></p> <p><u>U.S. Patent No. 7619912</u></p> <p>1:25-34; 2:46-3:28; 5:5-7:53; 21:36-24:58; 28:13-44; 31:24-31; Figures 1A, 1B, 2A, 2B, 3A, 10, 11A, 11B.</p>

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			<p>JEDEC standard JESD79D, "Double Data Rate (DDR) SDRAM Specification." published February 2004.</p> <p><u>File Histories</u></p> <p>File histories of U.S. Patents: No. 7619912, No. 7286436, No. 7289386, No. 7532537, No. 7636274, No. 8154901, No. 8001434, No. 8417870, No. 7864627, No. 7881150, No. 8516185, No. 7965578, No. 8081535, No. 7916574, No. 7965579, No. 8072837, No. 8081536, No. 8081537, No. 8359501, No. 8756364, No. 8516188, No. 8787060, No. 8782350, No. 8689064, No. 9128632, No. 9606907, No. 9037774, No. 10217523, No. 9037809, No. 9318160, No. 9858215, No. 9846659, No. 11093417, No. 10902886, No. 10860506, No. 10489314, No. 10268608, No. 10290328, No. 10949339, No. 9824035, No. 9659601, No. 9563587, No. 10025731, No. 61409893</p> <p>File histories of U.S. Patent Applications: No. 2022/0208233, No. 2021/0382834, No. 2021/0271593, No. 2021/0149829, No. 2019/0295675, No. 2021/0225415</p> <p><u>Inter Partes Reviews</u></p> <p>IPR2014-00882 (<i>see, e.g.</i>, POPR (Paper 9) at 5, 17), IPR2014-00883 (<i>see, e.g.</i>, POPR (Paper 8) at 5-7, 15; POR (Paper 25) at 26), IPR2014-00970, IPR2014-00971, IPR2014-01011, IPR2014-01029, IPR2014-01369, IPR2014-01370, IPR2014-01371, IPR2014-01372, IPR2014-01373, IPR2014-01374, IPR2014-01375, IPR2015-01020, IPR2015-01021, IPR2017-00548, IPR2017-00549, IPR2017-00560, IPR2017-00561, IPR2017-00562, IPR2017-00577, IPR2017-00587, IPR2017-00667, IPR2017-00668, IPR2017-00692, IPR2017-00730, IPR2018-00303, IPR2018-00362, IPR2018-00363, IPR2018-00364, IPR2018-00365, IPR2020-01042, IPR2020-01044, IPR2020-01421, IPR2022-00062, IPR2022-00063, IPR2022-00064, IPR2022-00236, IPR2022-00237, IPR2022-00615, IPR2022-00639, IPR2022-00711, IPR2022-00744, IPR2022-00745, IPR2022-00996, IPR2022-00999, IPR2022-01427, IPR2022-01428, IPR2023-00203, IPR2023-00204,</p>

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			<p>IPR2023-00205, IPR2023-00405, IPR2023-00406, IPR2023-00454, IPR2023-00455, IPR2023-00847, IPR2023-00883</p> <p><u>Inter Partes Reexaminations</u></p> <p>No. 95/000546, No. 95/000577, No. 95/000578, No. 95/000579, No. 95/001337, No. 95/001339, No. 95/001381, No. 95/001758</p> <p><u>Federal Circuit Appeals</u></p> <p>No. 15-126, No. 15-1179, No. 16-1742 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-1743 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-1744 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-2274, No. 16-2666, No. 17-1617, No. 17-1618, No. 18-1676, No. 18-2034, No. 18-2036, No. 18-2037, No. 18-2123, No. 18-2357, No. 19-1720, No. 19-2340, No. 20-1026, No. 21-113, No. 21-114</p> <p><u>Extrinsic Evidence</u></p> <p><u>District Court Cases</u></p> <p>No. 2:09-cv-06900 (C.D. Cal.), No. 8:13-cv-00996 (C.D. Cal.), No. 8:16-cv-01605 (C.D. Cal.), No. 8:17-cv-01030 (C.D. Cal.), No. 2:12-cv-02319 (E.D. Cal.), No. 2:13-cv-02613 (E.D. Cal.), No. 3:09-cv-05718 (N.D. Cal.), No. 4:08-cv-04144 (N.D. Cal.), No. 4:13-cv-03901 (N.D. Cal.), No. 4:13-cv-03916 (N.D. Cal.), No. 4:13-cv-05889 (N.D. Cal.), No. 4:13-cv-05962 (N.D. Cal.), No. 5:22-mc-80337 (N.D. Cal.), No. 1:09-cv-00165 (D. Del.), No. 1:21-cv-01453 (D. Del.), No. 2:21-cv-00463 (E.D. Tex.), No. 2:22-cv-00203 (E.D. Tex.), No. 2:22-cv-00294 (E.D. Tex.), No. 1:22-cv-00134 (W.D. Tex.), No. 1:22-cv-00136 (W.D. Tex.),</p>

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			<p>No. 6:20-cv-00194 (W.D. Tex.), No. 6:20-cv-00525 (W.D. Tex.), No. 6:21-cv-00430 (W.D. Tex.), No. 6:21-cv-00431 (W.D. Tex.)</p> <p><u>International Trade Commission Investigations</u></p> <p>No. 337-TA-1023, No. 337-TA-1089</p> <p><u>Others</u></p> <p>JEDEC Standards: JESD 205 Standard, JESD 82-20A Standard, JESD 206 Standard, JESD 79-2F Standard, JEDEC Standard No. 21C, JEDEC No. 21C Specification for DDR3 LRDIMM, JESD 82-30 Standard, JESD 79-3F Standard, JESD 248A Standard, JESD 79-4 Standard, JESD 82-31A Standard, JESD 79-4-1B Standard, JESD 79-4C Standard</p> <p>Memory Systems: Cache, DRAM, Disk (Bruce Jacob) (2008)</p> <p>Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob) (December 10, 2002)</p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '912 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p> <p>Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.</p>
26	'912: 1, 15, 28, 39	"wherein the logic element generates gated column access strobe (CAS)	"the logic element generates gated column access strobe signals or chip-select signals in response at least in part to all four of (i) the at least one row address signal, (ii) the bank

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
		<p>signals or chip-select signals of the output [control] signals in response at least in part to (i) the [at least one] row address signal, (ii) the bank address signals, and (iii) the [at least one] chip-select signal of the [set/plurality] of input [control] signals and (iv) the PLL clock signal”</p>	<p>address signals, (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal”</p> <p><u>Intrinsic Evidence</u></p> <p><u>U.S. Patent No. 7619912</u></p> <p>4:42-5:21; 6:55-9:21; 11:43-12:10; 12:12-23:25; 24:1-13; 26:1-27; Figs 1A, 1B, 2A, 2B, 3A, 3B, 11A, 11B.</p> <p>JEDEC standard JESD79D, “Double Data Rate (DDR) SDRAM Specification.” published February 2004.</p> <p><u>File Histories</u></p> <p>File histories of U.S. Patents: No. 7619912, No. 7286436, No. 7289386, No. 7532537, No. 7636274, No. 8154901, No. 8001434, No. 8417870, No. 7864627, No. 7881150, No. 8516185, No. 7965578, No. 8081535, No. 7916574, No. 7965579, No. 8072837, No. 8081536, No. 8081537, No. 8359501, No. 8756364, No. 8516188, No. 8787060, No. 8782350, No. 8689064, No. 9128632, No. 9606907, No. 9037774, No. 10217523, No. 9037809, No. 9318160, No. 9858215, No. 9846659, No. 11093417, No. 10902886, No. 10860506, No. 10489314, No. 10268608, No. 10290328, No. 10949339, No. 9824035, No. 9659601, No. 9563587, No. 10025731, No. 61409893</p> <p>File histories of U.S. Patent Applications: No. 2022/0208233, No. 2021/0382834, No. 2021/0271593, No. 2021/0149829, No. 2019/0295675, No. 2021/0225415</p> <p><u>Inter Partes Reviews</u></p> <p>IPR2014-00882 (<i>see, e.g.</i>, POPR (Paper 9) at 5, 17), IPR2014-00883 (<i>see, e.g.</i>, POPR (Paper 8) at 5-7, 15; POR (Paper 25) at 26), IPR2014-00970, IPR2014-00971, IPR2014-01011,</p>

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			<p>IPR2014-01029, IPR2014-01369, IPR2014-01370, IPR2014-01371, IPR2014-01372, IPR2014-01373, IPR2014-01374, IPR2014-01375, IPR2015-01020, IPR2015-01021, IPR2017-00548, IPR2017-00549, IPR2017-00560, IPR2017-00561, IPR2017-00562, IPR2017-00577, IPR2017-00587, IPR2017-00667, IPR2017-00668, IPR2017-00692, IPR2017-00730, IPR2018-00303, IPR2018-00362, IPR2018-00363, IPR2018-00364, IPR2018-00365, IPR2020-01042, IPR2020-01044, IPR2020-01421, IPR2022-00062, IPR2022-00063, IPR2022-00064, IPR2022-00236, IPR2022-00237, IPR2022-00615, IPR2022-00639, IPR2022-00711, IPR2022-00744, IPR2022-00745, IPR2022-00996, IPR2022-00999, IPR2022-01427, IPR2022-01428, IPR2023-00203, IPR2023-00204, IPR2023-00205, IPR2023-00405, IPR2023-00406, IPR2023-00454, IPR2023-00455, IPR2023-00847, IPR2023-00883</p> <p><u>Inter Partes Reexaminations</u></p> <p>No. 95/000546, No. 95/000577, No. 95/000578, No. 95/000579, No. 95/001337, No. 95/001339, No. 95/001381, No. 95/001758</p> <p><u>Federal Circuit Appeals</u></p> <p>No. 15-126, No. 15-1179, No. 16-1742 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-1743 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-1744 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-2274, No. 16-2666, No. 17-1617, No. 17-1618, No. 18-1676, No. 18-2034, No. 18-2036, No. 18-2037, No. 18-2123, No. 18-2357, No. 19-1720, No. 19-2340, No. 20-1026, No. 21-113, No. 21-114</p> <p><u>Extrinsic Evidence</u></p> <p><u>District Court Cases</u></p>

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			<p>No. 2:09-cv-06900 (C.D. Cal.), No. 8:13-cv-00996 (C.D. Cal.), No. 8:16-cv-01605 (C.D. Cal.), No. 8:17-cv-01030 (C.D. Cal.), No. 2:12-cv-02319 (E.D. Cal.), No. 2:13-cv-02613 (E.D. Cal.), No. 3:09-cv-05718 (N.D. Cal.), No. 4:08-cv-04144 (N.D. Cal.), No. 4:13-cv-03901 (N.D. Cal.), No. 4:13-cv-03916 (N.D. Cal.), No. 4:13-cv-05889 (N.D. Cal.), No. 4:13-cv-05962 (N.D. Cal.), No. 5:22-mc-80337 (N.D. Cal.), No. 1:09-cv-00165 (D. Del.), No. 1:21-cv-01453 (D. Del.), No. 2:21-cv-00463 (E.D. Tex.), No. 2:22-cv-00203 (E.D. Tex.), No. 2:22-cv-00294 (E.D. Tex.), No. 1:22-cv-00134 (W.D. Tex.), No. 1:22-cv-00136 (W.D. Tex.), No. 6:20-cv-00194 (W.D. Tex.), No. 6:20-cv-00525 (W.D. Tex.), No. 6:21-cv-00430 (W.D. Tex.), No. 6:21-cv-00431 (W.D. Tex.)</p> <p><u>International Trade Commission Investigations</u></p> <p>No. 337-TA-1023, No. 337-TA-1089</p> <p><u>Others</u></p> <p>JEDEC Standards: JESD 205 Standard, JESD 82-20A Standard, JESD 206 Standard, JESD 79-2F Standard, JEDEC Standard No. 21C, JEDEC No. 21C Specification for DDR3 LRDIMM, JESD 82-30 Standard, JESD 79-3F Standard, JESD 248A Standard, JESD 79-4 Standard, JESD 82-31A Standard, JESD 79-4-1B Standard, JESD 79-4C Standard</p> <p>Memory Systems: Cache, DRAM, Disk (Bruce Jacob) (2008)</p> <p>Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob) (December 10, 2002)</p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '912 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p>

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			<p>Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.</p>
27	'912: 77	<p>"wherein the logic element responds to at least (i) a row address bit of the at least one row/column address signal, (ii) the bank signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock by generating a first number of chip-select signals of the set of output control signals, the first number of chip-select signals generated by the logic element equal to the first number of ranks, and the at least one chip-select signal of the set of input control signals comprises a second number of chip-select signals equal to the second number of ranks"</p>	<p>"the logic element generates a number of chip-select signals equal to the first number of ranks in response to all four of (i) a row address bit of the at least one row/column address signal, (ii) the bank address signals, (iii) a number of chip-select signals of the set of input control signals equal to the second number of ranks and (iv) the PLL clock signal"</p> <p><u>Intrinsic Evidence</u></p> <p><u>U.S. Patent No. 7619912</u></p> <p>4:42-5:21; 6:55-9:21; 11:43-12:10; 12:12-23:25; 24:1-13; 26:1-27; Figs 1A, 1B, 2A, 2B, 3A, 3B, 11A, 11B.</p> <p>JEDEC standard JESD79D, "Double Data Rate (DDR) SDRAM Specification." published February 2004.</p> <p><u>File Histories</u></p> <p>File histories of U.S. Patents: No. 7619912, No. 7286436, No. 7289386, No. 7532537, No. 7636274, No. 8154901, No. 8001434, No. 8417870, No. 7864627, No. 7881150, No. 8516185, No. 7965578, No. 8081535, No. 7916574, No. 7965579, No. 8072837, No. 8081536, No. 8081537, No. 8359501, No. 8756364, No. 8516188, No. 8787060, No. 8782350, No. 8689064, No. 9128632, No. 9606907, No. 9037774, No. 10217523, No. 9037809, No. 9318160, No. 9858215, No. 9846659, No. 11093417, No. 10902886, No. 10860506, No. 10489314, No. 10268608, No. 10290328, No. 10949339, No. 9824035, No. 9659601, No. 9563587, No. 10025731, No. 61409893</p>

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28	'912: 80	<p>"wherein the generation of the first number of chip-select signals of the output control signals by the logic element is based on the logic element responsive at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals received by the logic element and (iv) the clock signals received from the phase-lock loop device"</p>	<p>"the logic element generates the first number of chip-select signals in response at least in part to all four of (i) the at least one row address signal, (ii) the bank address signals, (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal"</p> <p><u>Intrinsic Evidence</u></p> <p><u>U.S. Patent No. 7619912</u></p> <p>4:42-5:21; 6:55-9:21; 11:43-12:10; 12:12-23:25; 24:1-13; 26:1-27; Figs 1A, 1B, 2A, 2B, 3A, 3B, 11A, 11B.</p> <p>JEDEC standard JESD79D, "Double Data Rate (DDR) SDRAM Specification." published February 2004.</p> <p><u>File Histories</u></p> <p>File histories of U.S. Patents: No. 7619912, No. 7286436, No. 7289386, No. 7532537, No. 7636274, No. 8154901, No. 8001434, No. 8417870, No. 7864627, No. 7881150, No. 8516185, No. 7965578, No. 8081535, No. 7916574, No. 7965579, No. 8072837, No.</p>

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			<p>8081536, No. 8081537, No. 8359501, No. 8756364, No. 8516188, No. 8787060, No. 8782350, No. 8689064, No. 9128632, No. 9606907, No. 9037774, No. 10217523, No. 9037809, No. 9318160, No. 9858215, No. 9846659, No. 11093417, No. 10902886, No. 10860506, No. 10489314, No. 10268608, No. 10290328, No. 10949339, No. 9824035, No. 9659601, No. 9563587, No. 10025731, No. 61409893</p> <p><u>Inter Partes Reviews</u></p> <p>IPR2014-00882 (<i>see, e.g.</i>, POPR (Paper 9) at 5, 17), IPR2014-00883 (<i>see, e.g.</i>, POPR (Paper 8) at 5-7, 15; POR (Paper 25) at 26), IPR2014-00970, IPR2014-00971, IPR2014-01011, IPR2014-01029, IPR2014-01369, IPR2014-01370, IPR2014-01371, IPR2014-01372, IPR2014-01373, IPR2014-01374, IPR2014-01375, IPR2015-01020, IPR2015-01021, IPR2017-00548, IPR2017-00549, IPR2017-00560, IPR2017-00561, IPR2017-00562, IPR2017-00577, IPR2017-00587, IPR2017-00667, IPR2017-00668, IPR2017-00692, IPR2017-00730, IPR2018-00303, IPR2018-00362, IPR2018-00363, IPR2018-00364, IPR2018-00365, IPR2020-01042, IPR2020-01044, IPR2020-01421, IPR2022-00062, IPR2022-00063, IPR2022-00064, IPR2022-00236, IPR2022-00237, IPR2022-00615, IPR2022-00639, IPR2022-00711, IPR2022-00744, IPR2022-00745, IPR2022-00996, IPR2022-00999, IPR2022-01427, IPR2022-01428, IPR2023-00203, IPR2023-00204, IPR2023-00205, IPR2023-00405, IPR2023-00406, IPR2023-00454, IPR2023-00455, IPR2023-00847, IPR2023-00883</p> <p><u>Inter Partes Reexaminations</u></p> <p>No. 95/000546, No. 95/000577, No. 95/000578, No. 95/000579, No. 95/001337, No. 95/001339, No. 95/001381, No. 95/001758</p> <p><u>Federal Circuit Appeals</u></p> <p>No. 15-126, No. 15-1179, No. 16-1742 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-</p>

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
			<p>3), No. 16-1743 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-1744 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-2274, No. 16-2666, No. 17-1617, No. 17-1618, No. 18-1676, No. 18-2034, No. 18-2036, No. 18-2037, No. 18-2123, No. 18-2357, No. 19-1720, No. 19-2340, No. 20-1026, No. 21-113, No. 21-114</p> <p><u>Extrinsic Evidence</u></p> <p><u>District Court Cases</u></p> <p>No. 2:09-cv-06900 (C.D. Cal.), No. 8:13-cv-00996 (C.D. Cal.), No. 8:16-cv-01605 (C.D. Cal.), No. 8:17-cv-01030 (C.D. Cal.), No. 2:12-cv-02319 (E.D. Cal.), No. 2:13-cv-02613 (E.D. Cal.), No. 3:09-cv-05718 (N.D. Cal.), No. 4:08-cv-04144 (N.D. Cal.), No. 4:13-cv-03901 (N.D. Cal.), No. 4:13-cv-03916 (N.D. Cal.), No. 4:13-cv-05889 (N.D. Cal.), No. 4:13-cv-05962 (N.D. Cal.), No. 5:22-mc-80337 (N.D. Cal.), No. 1:09-cv-00165 (D. Del.), No. 1:21-cv-01453 (D. Del.), No. 2:21-cv-00463 (E.D. Tex.), No. 2:22-cv-00203 (E.D. Tex.), No. 2:22-cv-00294 (E.D. Tex.), No. 1:22-cv-00134 (W.D. Tex.), No. 1:22-cv-00136 (W.D. Tex.), No. 6:20-cv-00194 (W.D. Tex.), No. 6:20-cv-00525 (W.D. Tex.), No. 6:21-cv-00430 (W.D. Tex.), No. 6:21-cv-00431 (W.D. Tex.)</p> <p><u>International Trade Commission Investigations</u></p> <p>No. 337-TA-1023, No. 337-TA-1089</p> <p><u>Others</u></p> <p>JEDEC Standards: JESD 205 Standard, JESD 82-20A Standard, JESD 206 Standard, JESD 79-2F Standard, JEDEC Standard No. 21C, JEDEC No. 21C Specification for DDR3 LRDIMM, JESD 82-30 Standard, JESD 79-3F Standard, JESD 248A Standard, JESD 79-4 Standard, JESD 82-31A Standard, JESD 79-4-1B Standard, JESD 79-4C Standard</p>

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
			<p>Memory Systems: Cache, DRAM, Disk (Bruce Jacob) (2008)</p> <p>Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob) (December 10, 2002)</p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '912 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p> <p>Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.</p>
29	'912: 82, 86	<p>"wherein the logic element responds to at least the at least one row address signal, the bank address signals, and the at least one chip-select signal of the set of input [control] signals and the PLL clock signal by generating a number of rank-selecting signals of the set of output [control] signals that is greater than double or equal to double the number of chip-select signals of the set of input [control] signals"</p>	<p>"the logic element generates a number of rank-selecting signals greater than or equal to double the number of input chip-select signals in response to all four of (i) the at least one row address signal, (ii) the bank address signals, (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal"</p> <p><u>Intrinsic Evidence</u></p> <p><u>U.S. Patent No. 7619912</u></p> <p>4:42-5:21; 6:55-9:21; 11:43-12:10; 12:12-23:25; 24:1-13; 26:1-27; Figs 1A, 1B, 2A, 2B, 3A, 3B, 11A, 11B.</p> <p>JEDEC standard JESD79D, "Double Data Rate (DDR) SDRAM Specification." published February 2004.</p> <p><u>File Histories</u></p>

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			<p>File histories of U.S. Patents: No. 7619912, No. 7286436, No. 7289386, No. 7532537, No. 7636274, No. 8154901, No. 8001434, No. 8417870, No. 7864627, No. 7881150, No. 8516185, No. 7965578, No. 8081535, No. 7916574, No. 7965579, No. 8072837, No. 8081536, No. 8081537, No. 8359501, No. 8756364, No. 8516188, No. 8787060, No. 8782350, No. 8689064, No. 9128632, No. 9606907, No. 9037774, No. 10217523, No. 9037809, No. 9318160, No. 9858215, No. 9846659, No. 11093417, No. 10902886, No. 10860506, No. 10489314, No. 10268608, No. 10290328, No. 10949339, No. 9824035, No. 9659601, No. 9563587, No. 10025731, No. 61409893</p> <p>File histories of U.S. Patent Applications: No. 2022/0208233, No. 2021/0382834, No. 2021/0271593, No. 2021/0149829, No. 2019/0295675, No. 2021/0225415</p> <p><u>Inter Partes Reviews</u></p> <p>IPR2014-00882 (<i>see, e.g.</i>, POPR (Paper 9) at 5, 17), IPR2014-00883 (<i>see, e.g.</i>, POPR (Paper 8) at 5-7, 15; POR (Paper 25) at 26), IPR2014-00970, IPR2014-00971, IPR2014-01011, IPR2014-01029, IPR2014-01369, IPR2014-01370, IPR2014-01371, IPR2014-01372, IPR2014-01373, IPR2014-01374, IPR2014-01375, IPR2015-01020, IPR2015-01021, IPR2017-00548, IPR2017-00549, IPR2017-00560, IPR2017-00561, IPR2017-00562, IPR2017-00577, IPR2017-00587, IPR2017-00667, IPR2017-00668, IPR2017-00692, IPR2017-00730, IPR2018-00303, IPR2018-00362, IPR2018-00363, IPR2018-00364, IPR2018-00365, IPR2020-01042, IPR2020-01044, IPR2020-01421, IPR2022-00062, IPR2022-00063, IPR2022-00064, IPR2022-00236, IPR2022-00237, IPR2022-00615, IPR2022-00639, IPR2022-00711, IPR2022-00744, IPR2022-00745, IPR2022-00996, IPR2022-00999, IPR2022-01427, IPR2022-01428, IPR2023-00203, IPR2023-00204, IPR2023-00205, IPR2023-00405, IPR2023-00406, IPR2023-00454, IPR2023-00455, IPR2023-00847, IPR2023-00883</p> <p><u>Inter Partes Reexaminations</u></p>

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
			<p>No. 95/000546, No. 95/000577, No. 95/000578, No. 95/000579, No. 95/001337, No. 95/001339, No. 95/001381, No. 95/001758</p> <p><u>Federal Circuit Appeals</u></p> <p>No. 15-126, No. 15-1179, No. 16-1742 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-1743 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-1744 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-2274, No. 16-2666, No. 17-1617, No. 17-1618, No. 18-1676, No. 18-2034, No. 18-2036, No. 18-2037, No. 18-2123, No. 18-2357, No. 19-1720, No. 19-2340, No. 20-1026, No. 21-113, No. 21-114</p> <p><u>Extrinsic Evidence</u></p> <p><u>District Court Cases</u></p> <p>No. 2:09-cv-06900 (C.D. Cal.), No. 8:13-cv-00996 (C.D. Cal.), No. 8:16-cv-01605 (C.D. Cal.), No. 8:17-cv-01030 (C.D. Cal.), No. 2:12-cv-02319 (E.D. Cal.), No. 2:13-cv-02613 (E.D. Cal.), No. 3:09-cv-05718 (N.D. Cal.), No. 4:08-cv-04144 (N.D. Cal.), No. 4:13-cv-03901 (N.D. Cal.), No. 4:13-cv-03916 (N.D. Cal.), No. 4:13-cv-05889 (N.D. Cal.), No. 4:13-cv-05962 (N.D. Cal.), No. 5:22-mc-80337 (N.D. Cal.), No. 1:09-cv-00165 (D. Del.), No. 1:21-cv-01453 (D. Del.), No. 2:21-cv-00463 (E.D. Tex.), No. 2:22-cv-00203 (E.D. Tex.), No. 2:22-cv-00294 (E.D. Tex.), No. 1:22-cv-00134 (W.D. Tex.), No. 1:22-cv-00136 (W.D. Tex.), No. 6:20-cv-00194 (W.D. Tex.), No. 6:20-cv-00525 (W.D. Tex.), No. 6:21-cv-00430 (W.D. Tex.), No. 6:21-cv-00431 (W.D. Tex.)</p> <p><u>International Trade Commission Investigations</u></p> <p>No. 337-TA-1023, No. 337-TA-1089</p>

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
			<p><u>Others</u></p> <p>JEDEC Standards: JESD 205 Standard, JESD 82-20A Standard, JESD 206 Standard, JESD 79-2F Standard, JEDEC Standard No. 21C, JEDEC No. 21C Specification for DDR3 LRDIMM, JESD 82-30 Standard, JESD 79-3F Standard, JESD 248A Standard, JESD 79-4 Standard, JESD 82-31A Standard, JESD 79-4-1B Standard, JESD 79-4C Standard</p> <p>Memory Systems: Cache, DRAM, Disk (Bruce Jacob) (2008)</p> <p>Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob) (December 10, 2002)</p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '912 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p> <p>Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.</p>
30	'912: 88	<p>"wherein the logic element responds to at least (i) the row address signal, (ii) the bank address signals, (iii) and the one chip-select signal of the set of input control signals and (iv) the PLL clock signal by generating a number of</p>	<p>"the logic element generates a number of rank-selecting signals greater than or equal to double the number of input chip-select signals in response to all four of (i) the at least one row address signal, (ii) the bank address signals, (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal"</p> <p><u>Intrinsic Evidence</u></p> <p><u>U.S. Patent No. 7619912</u></p>

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
		rank-selecting signals of the set of output signals that is greater than double or equal to double the number of chip-select signals of the set of input control signals”	<p>4:42-5:21; 6:55-9:21; 11:43-12:10; 12:12-23:25; 24:1-13; 26:1-27; Figs 1A, 1B, 2A, 2B, 3A, 3B, 11A, 11B.</p> <p>JEDEC standard JESD79D, “Double Data Rate (DDR) SDRAM Specification.” published February 2004.</p> <p><u>File Histories</u></p> <p>File histories of U.S. Patents: No. 7619912, No. 7286436, No. 7289386, No. 7532537, No. 7636274, No. 8154901, No. 8001434, No. 8417870, No. 7864627, No. 7881150, No. 8516185, No. 7965578, No. 8081535, No. 7916574, No. 7965579, No. 8072837, No. 8081536, No. 8081537, No. 8359501, No. 8756364, No. 8516188, No. 8787060, No. 8782350, No. 8689064, No. 9128632, No. 9606907, No. 9037774, No. 10217523, No. 9037809, No. 9318160, No. 9858215, No. 9846659, No. 11093417, No. 10902886, No. 10860506, No. 10489314, No. 10268608, No. 10290328, No. 10949339, No. 9824035, No. 9659601, No. 9563587, No. 10025731, No. 61409893</p> <p>File histories of U.S. Patent Applications: No. 2022/0208233, No. 2021/0382834, No. 2021/0271593, No. 2021/0149829, No. 2019/0295675, No. 2021/0225415</p> <p><u>Inter Partes Reviews</u></p> <p>IPR2014-00882 (<i>see, e.g.</i>, POPR (Paper 9) at 5, 17), IPR2014-00883 (<i>see, e.g.</i>, POPR (Paper 8) at 5-7, 15; POR (Paper 25) at 26), IPR2014-00970, IPR2014-00971, IPR2014-01011, IPR2014-01029, IPR2014-01369, IPR2014-01370, IPR2014-01371, IPR2014-01372, IPR2014-01373, IPR2014-01374, IPR2014-01375, IPR2015-01020, IPR2015-01021, IPR2017-00548, IPR2017-00549, IPR2017-00560, IPR2017-00561, IPR2017-00562, IPR2017-00577, IPR2017-00587, IPR2017-00667, IPR2017-00668, IPR2017-00692, IPR2017-00730, IPR2018-00303, IPR2018-00362, IPR2018-00363, IPR2018-00364, IPR2018-00365, IPR2020-01042, IPR2020-01044, IPR2020-01421, IPR2022-00062, IPR2022-00063, IPR2022-00064, IPR2022-00236, IPR2022-00237, IPR2022-00615,</p>

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
			<p>IPR2022-00639, IPR2022-00711, IPR2022-00744, IPR2022-00745, IPR2022-00996, IPR2022-00999, IPR2022-01427, IPR2022-01428, IPR2023-00203, IPR2023-00204, IPR2023-00205, IPR2023-00405, IPR2023-00406, IPR2023-00454, IPR2023-00455, IPR2023-00847, IPR2023-00883</p> <p><u>Inter Partes Reexaminations</u></p> <p>No. 95/000546, No. 95/000577, No. 95/000578, No. 95/000579, No. 95/001337, No. 95/001339, No. 95/001381, No. 95/001758</p> <p><u>Federal Circuit Appeals</u></p> <p>No. 15-126, No. 15-1179, No. 16-1742 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-1743 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-1744 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-2274, No. 16-2666, No. 17-1617, No. 17-1618, No. 18-1676, No. 18-2034, No. 18-2036, No. 18-2037, No. 18-2123, No. 18-2357, No. 19-1720, No. 19-2340, No. 20-1026, No. 21-113, No. 21-114</p> <p><u>Extrinsic Evidence</u></p> <p><u>District Court Cases</u></p> <p>No. 2:09-cv-06900 (C.D. Cal.), No. 8:13-cv-00996 (C.D. Cal.), No. 8:16-cv-01605 (C.D. Cal.), No. 8:17-cv-01030 (C.D. Cal.), No. 2:12-cv-02319 (E.D. Cal.), No. 2:13-cv-02613 (E.D. Cal.), No. 3:09-cv-05718 (N.D. Cal.), No. 4:08-cv-04144 (N.D. Cal.), No. 4:13-cv-03901 (N.D. Cal.), No. 4:13-cv-03916 (N.D. Cal.), No. 4:13-cv-05889 (N.D. Cal.), No. 4:13-cv-05962 (N.D. Cal.), No. 5:22-mc-80337 (N.D. Cal.), No. 1:09-cv-00165 (D. Del.), No. 1:21-cv-01453 (D. Del.), No. 2:21-cv-00463 (E.D. Tex.), No. 2:22-cv-00203 (E.D. Tex.), No.</p>

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
			<p>2:22-cv-00294 (E.D. Tex.), No. 1:22-cv-00134 (W.D. Tex.), No. 1:22-cv-00136 (W.D. Tex.), No. 6:20-cv-00194 (W.D. Tex.), No. 6:20-cv-00525 (W.D. Tex.), No. 6:21-cv-00430 (W.D. Tex.), No. 6:21-cv-00431 (W.D. Tex.)</p> <p><u>International Trade Commission Investigations</u></p> <p>No. 337-TA-1023, No. 337-TA-1089</p> <p><u>Others</u></p> <p>JEDEC Standards: JESD 205 Standard, JESD 82-20A Standard, JESD 206 Standard, JESD 79-2F Standard, JEDEC Standard No. 21C, JEDEC No. 21C Specification for DDR3 LRDIMM, JESD 82-30 Standard, JESD 79-3F Standard, JESD 248A Standard, JESD 79-4 Standard, JESD 82-31A Standard, JESD 79-4-1B Standard, JESD 79-4C Standard</p> <p>Memory Systems: Cache, DRAM, Disk (Bruce Jacob) (2008)</p> <p>Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob) (December 10, 2002)</p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '912 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p> <p>Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.</p>
31	'912: 90	"wherein the logic element responds to at least (i) the	"the logic element generates a number of chip select signals greater than or equal to double the number of input chip-select signals in response to all of (i) the at least one row

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		<p>at least one row signal, (ii) the bank address signals, (iii) and the second number of chip-select signals of the plurality of input signals and (iv) the PLL clock signal by generating the first number of chip-select signals of the plurality of output signals that is greater than double or equal to double the second number of chip-select signals of the plurality of input signals”</p>	<p>address signal, (ii) the bank address signals, (iii) the second number of chip-select signals of the set of input control signals and (iv) the PLL clock signal”</p> <p><u>Intrinsic Evidence</u></p> <p><u>U.S. Patent No. 7619912</u></p> <p>4:42-5:21; 6:55-9:21; 11:43-12:10; 12:12-23:25; 24:1-13; 26:1-27; Figs 1A, 1B, 2A, 2B, 3A, 3B, 11A, 11B.</p> <p>JEDEC standard JESD79D, “Double Data Rate (DDR) SDRAM Specification.” published February 2004.</p> <p><u>File Histories</u></p> <p>File histories of U.S. Patents: No. 7619912, No. 7286436, No. 7289386, No. 7532537, No. 7636274, No. 8154901, No. 8001434, No. 8417870, No. 7864627, No. 7881150, No. 8516185, No. 7965578, No. 8081535, No. 7916574, No. 7965579, No. 8072837, No. 8081536, No. 8081537, No. 8359501, No. 8756364, No. 8516188, No. 8787060, No. 8782350, No. 8689064, No. 9128632, No. 9606907, No. 9037774, No. 10217523, No. 9037809, No. 9318160, No. 9858215, No. 9846659, No. 11093417, No. 10902886, No. 10860506, No. 10489314, No. 10268608, No. 10290328, No. 10949339, No. 9824035, No. 9659601, No. 9563587, No. 10025731, No. 61409893</p> <p>File histories of U.S. Patent Applications: No. 2022/0208233, No. 2021/0382834, No. 2021/0271593, No. 2021/0149829, No. 2019/0295675, No. 2021/0225415</p> <p><u>Inter Partes Reviews</u></p> <p>IPR2014-00882 (<i>see, e.g.</i>, POPR (Paper 9) at 5, 17), IPR2014-00883 (<i>see, e.g.</i>, POPR (Paper 8) at 5-7, 15; POR (Paper 25) at 26), IPR2014-00970, IPR2014-00971, IPR2014-01011,</p>

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			<p>IPR2014-01029, IPR2014-01369, IPR2014-01370, IPR2014-01371, IPR2014-01372, IPR2014-01373, IPR2014-01374, IPR2014-01375, IPR2015-01020, IPR2015-01021, IPR2017-00548, IPR2017-00549, IPR2017-00560, IPR2017-00561, IPR2017-00562, IPR2017-00577, IPR2017-00587, IPR2017-00667, IPR2017-00668, IPR2017-00692, IPR2017-00730, IPR2018-00303, IPR2018-00362, IPR2018-00363, IPR2018-00364, IPR2018-00365, IPR2020-01042, IPR2020-01044, IPR2020-01421, IPR2022-00062, IPR2022-00063, IPR2022-00064, IPR2022-00236, IPR2022-00237, IPR2022-00615, IPR2022-00639, IPR2022-00711, IPR2022-00744, IPR2022-00745, IPR2022-00996, IPR2022-00999, IPR2022-01427, IPR2022-01428, IPR2023-00203, IPR2023-00204, IPR2023-00205, IPR2023-00405, IPR2023-00406, IPR2023-00454, IPR2023-00455, IPR2023-00847, IPR2023-00883</p> <p><u>Inter Partes Reexaminations</u></p> <p>No. 95/000546, No. 95/000577, No. 95/000578, No. 95/000579, No. 95/001337, No. 95/001339, No. 95/001381, No. 95/001758</p> <p><u>Federal Circuit Appeals</u></p> <p>No. 15-126, No. 15-1179, No. 16-1742 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-1743 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-1744 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-2274, No. 16-2666, No. 17-1617, No. 17-1618, No. 18-1676, No. 18-2034, No. 18-2036, No. 18-2037, No. 18-2123, No. 18-2357, No. 19-1720, No. 19-2340, No. 20-1026, No. 21-113, No. 21-114</p> <p><u>Extrinsic Evidence</u></p> <p><u>District Court Cases</u></p>

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
			<p>No. 2:09-cv-06900 (C.D. Cal.), No. 8:13-cv-00996 (C.D. Cal.), No. 8:16-cv-01605 (C.D. Cal.), No. 8:17-cv-01030 (C.D. Cal.), No. 2:12-cv-02319 (E.D. Cal.), No. 2:13-cv-02613 (E.D. Cal.), No. 3:09-cv-05718 (N.D. Cal.), No. 4:08-cv-04144 (N.D. Cal.), No. 4:13-cv-03901 (N.D. Cal.), No. 4:13-cv-03916 (N.D. Cal.), No. 4:13-cv-05889 (N.D. Cal.), No. 4:13-cv-05962 (N.D. Cal.), No. 5:22-mc-80337 (N.D. Cal.), No. 1:09-cv-00165 (D. Del.), No. 1:21-cv-01453 (D. Del.), No. 2:21-cv-00463 (E.D. Tex.), No. 2:22-cv-00203 (E.D. Tex.), No. 2:22-cv-00294 (E.D. Tex.), No. 1:22-cv-00134 (W.D. Tex.), No. 1:22-cv-00136 (W.D. Tex.), No. 6:20-cv-00194 (W.D. Tex.), No. 6:20-cv-00525 (W.D. Tex.), No. 6:21-cv-00430 (W.D. Tex.), No. 6:21-cv-00431 (W.D. Tex.)</p> <p><u>International Trade Commission Investigations</u></p> <p>No. 337-TA-1023, No. 337-TA-1089</p> <p><u>Others</u></p> <p>JEDEC Standards: JESD 205 Standard, JESD 82-20A Standard, JESD 206 Standard, JESD 79-2F Standard, JEDEC Standard No. 21C, JEDEC No. 21C Specification for DDR3 LRDIMM, JESD 82-30 Standard, JESD 79-3F Standard, JESD 248A Standard, JESD 79-4 Standard, JESD 82-31A Standard, JESD 79-4-1B Standard, JESD 79-4C Standard</p> <p>Memory Systems: Cache, DRAM, Disk (Bruce Jacob) (2008)</p> <p>Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob) (December 10, 2002)</p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '912 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p>

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			<p>Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.</p>
32	'912: All Asserted Claims	"A memory module connectable to a computer system, the memory module comprising"	<p>Preamble not limiting.</p> <p>Plain and ordinary meaning.</p> <p><u>Intrinsic Evidence</u></p> <p><u>U.S. Patent No. 7619912</u></p> <p>Abstract; 2:46-3:28; 5:6-21; Figures 1A, 1B, 2A, 2B, 11A, 11B.</p> <p>JEDEC standard JESD79D, "Double Data Rate (DDR) SDRAM Specification." published February 2004.</p> <p><u>Extrinsic Evidence</u></p> <p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '912 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p> <p>Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.</p>
33	'912: All Asserted	"signal"	"a varying electrical impulse that conveys information from one point to another"

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
	Claims		<p><u>Intrinsic Evidence</u></p> <p><u>U.S. Patent No. 7619912</u></p> <p>2:34-3:28; 5:6-45; 6:55-12:10; 12:12-23:25; 23:27-25:67; 26:1-32:26; Figs 1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 5.</p> <p>JEDEC standard JESD79D, "Double Data Rate (DDR) SDRAM Specification." published February 2004.</p> <p><u>File Histories</u></p> <p>File histories of U.S. Patents: No. 7619912, No. 7286436, No. 7289386, No. 7532537, No. 7636274, No. 8154901, No. 8001434, No. 8417870, No. 7864627, No. 7881150, No. 8516185, No. 7965578, No. 8081535, No. 7916574, No. 7965579, No. 8072837, No. 8081536, No. 8081537, No. 8359501, No. 8756364, No. 8516188, No. 8787060, No. 8782350, No. 8689064, No. 9128632, No. 9606907, No. 9037774, No. 10217523, No. 9037809, No. 9318160, No. 9858215, No. 9846659, No. 11093417, No. 10902886, No. 10860506, No. 10489314, No. 10268608, No. 10290328, No. 10949339, No. 9824035, No. 9659601, No. 9563587, No. 10025731, No. 61409893</p> <p>File histories of U.S. Patent Applications: No. 2022/0208233, No. 2021/0382834, No. 2021/0271593, No. 2021/0149829, No. 2019/0295675, No. 2021/0225415</p> <p><u>Inter Partes Reviews</u></p> <p>IPR2014-00882 (<i>see, e.g.</i>, POPR (Paper 9) at 5, 17), IPR2014-00883 (<i>see, e.g.</i>, POPR (Paper 8) at 5-7, 15; POR (Paper 25) at 26), IPR2014-00970, IPR2014-00971, IPR2014-01011, IPR2014-01029, IPR2014-01369, IPR2014-01370, IPR2014-01371, IPR2014-01372, IPR2014-01373, IPR2014-01374, IPR2014-01375, IPR2015-01020, IPR2015-01021, IPR2017-00548, IPR2017-00549, IPR2017-00560, IPR2017-00561, IPR2017-00562,</p>

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			<p>IPR2017-00577, IPR2017-00587, IPR2017-00667, IPR2017-00668, IPR2017-00692, IPR2017-00730, IPR2018-00303, IPR2018-00362, IPR2018-00363, IPR2018-00364, IPR2018-00365, IPR2020-01042, IPR2020-01044, IPR2020-01421, IPR2022-00062, IPR2022-00063, IPR2022-00064, IPR2022-00236, IPR2022-00237, IPR2022-00615, IPR2022-00639, IPR2022-00711, IPR2022-00744, IPR2022-00745, IPR2022-00996, IPR2022-00999, IPR2022-01427, IPR2022-01428, IPR2023-00203, IPR2023-00204, IPR2023-00205, IPR2023-00405, IPR2023-00406, IPR2023-00454, IPR2023-00455, IPR2023-00847, IPR2023-00883</p> <p><u>Inter Partes Reexaminations</u></p> <p>No. 95/000546, No. 95/000577, No. 95/000578, No. 95/000579, No. 95/001337, No. 95/001339, No. 95/001381, No. 95/001758</p> <p><u>Federal Circuit Appeals</u></p> <p>No. 15-126, No. 15-1179, No. 16-1742 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-1743 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-1744 (<i>see, e.g.</i>, Netlist Opening Brief (Dkt. No. 20) at 8-13, 30, 40-46; Netlist Reply Brief (Dkt. No. 32) at 15; Opinion and Judgment (Dkt. No. 44) at 2-3), No. 16-2274, No. 16-2666, No. 17-1617, No. 17-1618, No. 18-1676, No. 18-2034, No. 18-2036, No. 18-2037, No. 18-2123, No. 18-2357, No. 19-1720, No. 19-2340, No. 20-1026, No. 21-113, No. 21-114</p> <p><u>Extrinsic Evidence</u></p> <p><u>District Court Cases</u></p> <p>No. 2:09-cv-06900 (C.D. Cal.), No. 8:13-cv-00996 (C.D. Cal.), No. 8:16-cv-01605 (C.D. Cal.), No. 8:17-cv-01030 (C.D. Cal.), No. 2:12-cv-02319 (E.D. Cal.), No. 2:13-cv-02613</p>

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			<p>(E.D. Cal.), No. 3:09-cv-05718 (N.D. Cal.), No. 4:08-cv-04144 (N.D. Cal.), No. 4:13-cv-03901 (N.D. Cal.), No. 4:13-cv-03916 (N.D. Cal.), No. 4:13-cv-05889 (N.D. Cal.), No. 4:13-cv-05962 (N.D. Cal.), No. 5:22-mc-80337 (N.D. Cal.), No. 1:09-cv-00165 (D. Del.), No. 1:21-cv-01453 (D. Del.), No. 2:21-cv-00463 (E.D. Tex.), No. 2:22-cv-00203 (E.D. Tex.), No. 2:22-cv-00294 (E.D. Tex.), No. 1:22-cv-00134 (W.D. Tex.), No. 1:22-cv-00136 (W.D. Tex.), No. 6:20-cv-00194 (W.D. Tex.), No. 6:20-cv-00525 (W.D. Tex.), No. 6:21-cv-00430 (W.D. Tex.), No. 6:21-cv-00431 (W.D. Tex.)</p> <p><u>International Trade Commission Investigations</u></p> <p>No. 337-TA-1023, No. 337-TA-1089</p> <p><u>Others</u></p> <p>JEDEC Standards: JESD 205 Standard, JESD 82-20A Standard, JESD 206 Standard, JESD 79-2F Standard, JEDEC Standard No. 21C, JEDEC No. 21C Specification for DDR3 LRDIMM, JESD 82-30 Standard, JESD 79-3F Standard, JESD 248A Standard, JESD 79-4 Standard, JESD 82-31A Standard, JESD 79-4-1B Standard, JESD 79-4C Standard</p> <p>Memory Systems: Cache, DRAM, Disk (Bruce Jacob) (2008)</p> <p>Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob) (December 10, 2002)</p> <p>The Penguin Dictionary of Electronics ("signal")</p> <p>Collins Dictionary Electronics: Definitions for the Digital Age ("signal")</p> <p>Microsoft Computer Dictionary, Fifth edition 2002 ("signal")</p>

#	Claim(s)	Terms for Construction	Samsung's Proposed Construction
			<p>Samsung may rely on testimony of Mr. Joe McAlexander and/or Dr. Paul Min to explain the technology, the state of the art at the time the application leading to the '912 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the alleged invention.</p> <p>Samsung may also rely on Mr. McAlexander and/or Dr. Min to respond to Netlist's and/or Micron's claim construction positions and any testimony of Netlist's and/or Micron's expert(s) and witnesses.</p>